

MS-7635 Ver: 1.0

uATX(244mm X 244mm), 4 layers

CPU:

INTEL - Lynnfield / Clarkdale LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH (H - 55)

OnBoard Chipset:

Clock Gen:ICS 4116

IDE X1 / e-SATA X1: JMB-363

HD Audio Codec:RTL889

LAN:RTL8111D 10/100/1000

SIO:FIN71889ED-LXA

Flash ROM: 64 Mb(by intel Spec.)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) X16 Slot * 1

PCI Express (X4) X16 Slot * 1

PCI Express (X1) X1 Slot * 1

PCI Slot *1

PWM: Controller: uP6213 -- CPU(4-Phase use 6X6 Dr. MOS -- 95W)
ISL6314 (GFX) -- OV by 6263

OV by SIO

uP6103A (CPU_VTT)

uP6103 (PCH)

uP6103 (DDR)

ACPI: uPI

Other:

SATA(SATA2-300MB/s) *6

USB2.0 *12 (Rear*6 / Front*6)

PRINT Header *1

COM PORT *1

TPM Header *1

on BOARD BUZZER

D-SUB *1

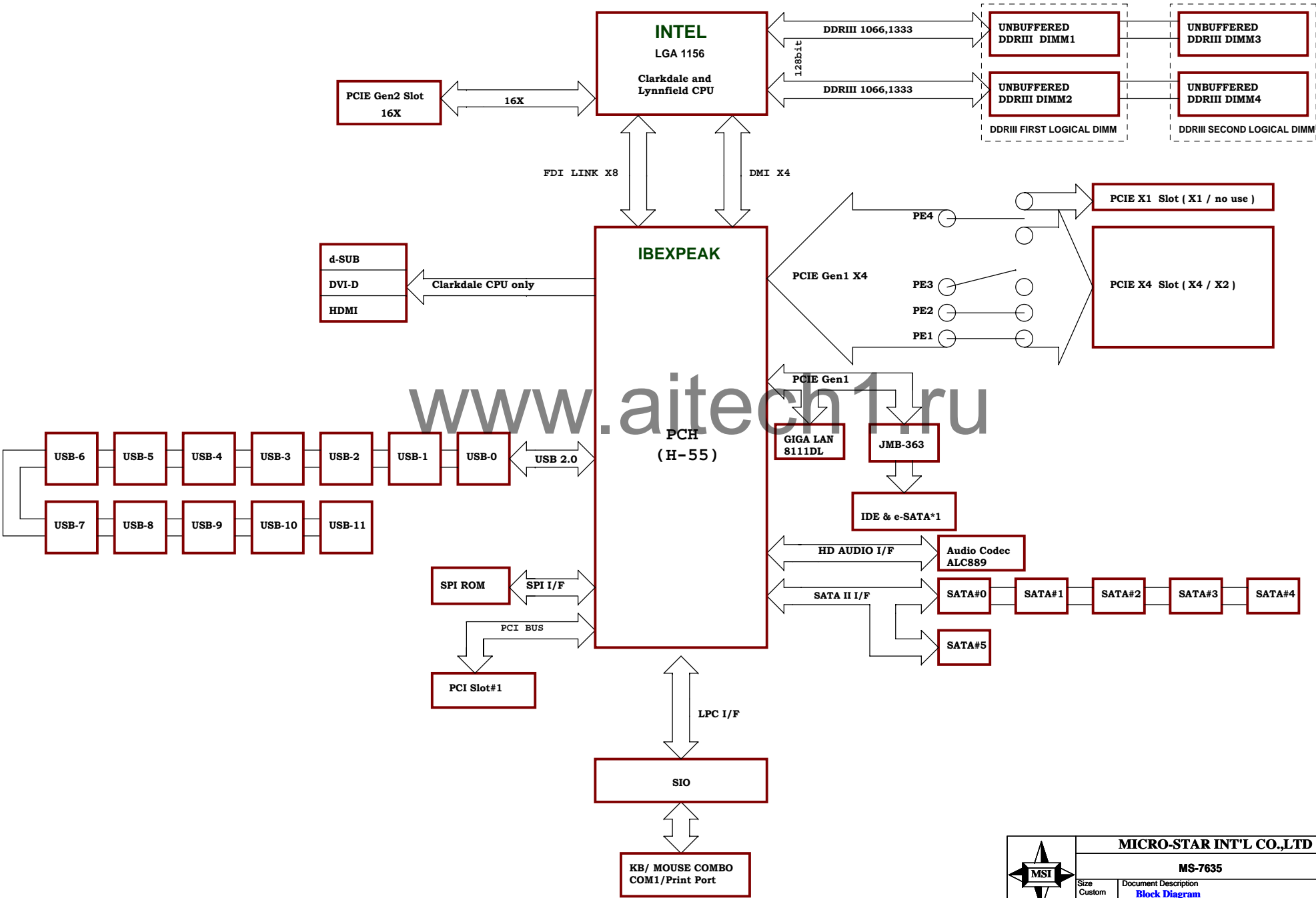
DVI-D PORT*1

HDMI *1

IDE *1

e-SATA *1

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	PCH CLKOUT_PCI<0>
TPM				PCH CLKOUT_PCI<3>
SIO				PCH CLKOUT_PCI<2>

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USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #4	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE IBEXPEAK

Signals	Target
PLTRST#	LPC/SIO & CPU & XDP
PLTRST_BU1#	JMB-363
PLTRST_BU2#	ALL PCI-E SLOT
PLTRST_BU3#	LAN & TPM
PCIRST#	PCI SLOT



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GPIO	Alt Func	Power	Tol	Default	Signal Name
GPIO[0]	UNMUXED	Core	3.3V	GPI	BM_BUSY#
GPIO[1]	TACH1	Core	3.3V	GPI	SYS1_FANTAC
GPIO[2]	PIRQE	Core	5V	GPI	PIRQE
GPIO[3]	PIRQF	Core	5V	GPI	PIRQF
GPIO[4]	PIRQG	Core	5V	GPI	PIRQG
GPIO[5]	PIRQH	Core	5V	GPI	PIRQH
GPIO[6]	TACH2	Core	3.3V	GPI	SYS2_FANTAC
GPIO[7]	TACH3	Core	3.3V	GPI	
GPIO[8]	UNMUXED	Resume	3.3V	GPI	
GPIO[9]	OC5#	Resume	3.3V	Native	OC5#
GPIO[10]	OC6#	Resume	3.3V	GPI	OC6#
GPIO[11]	SMBALERT#	Resume	3.3V	Native	
GPIO[12]	LAN_PHY_PWR_CTRL	Resume	3.3V	Native	
GPIO[13]	SIO_PME#	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	OC7#	Resume	3.3V	GPI	
GPIO[15]	UNMUXED	Resume	3.3V	GPI	SIO_HOLD_GPO#
GPIO[16]	SATA4GP	Core	3.3V	Native	
GPIO[17]	TACH0	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	PCIECLKRQ1#	Core	3.3V	GPO	
GPIO[19]	SATA1GP	Core	3.3V	GPI	
GPIO[20]	PCIECLKRQ2#	Core	3.3V	GPO	
GPIO[21]	SATA0GP	Core	3.3V	GPI	
GPIO[22]	SCLOCK	Core	3.3V	GPI	
GPIO[23]	LDRQ1	Core	3.3V	Native	
GPIO[24]	UNMUXED	Resume	3.3V	GPO	TURBO_MODE#
GPIO[25]	PCIECLKRQ3#	Resume	3.3V	Native	
GPIO[26]	PCIECLKRQ4#	Resume	3.3V	GPO	
GPIO[27]	UNMUXED	Resume	3.3V	GPO	
GPIO[28]	UNMUXED	Resume	3.3V	GPO	
GPIO[29]	SLP_LAN#	Resume	3.3V	Native	
GPIO[30]	PROC_MISSING	Resume	3.3V	GPO	
GPIO[31]	UNMUXED	Resume	3.3V	GPO	
GPIO[32]	UNMUXED	Core	3.3V	GPO	SPI_WP#
GPIO[33]	UNMUXED	Core	3.3V	GPO	
GPIO[34]	STP_PCI#	Core	3.3V	GPO	
GPIO[35]	UNMUXED	Core	3.3V	GPO	
GPIO[36]	SATA2GP	Core	3.3V	GPI	
GPIO[37]	SATA3GP	Core	3.3V	GPI	
GPIO[38]	SLOAD	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	Core	3.3V	GPI	
GPIO[40]	OC1#	Resume	3.3V	Native	OC1#
GPIO[41]	OC2#	Resume	3.3V	Native	OC2#
GPIO[42]	OC3#	Resume	3.3V	Native	OC3#
GPIO[43]	OC4#	Resume	3.3V	Native	OC4#
GPIO[44]	PCIECLKRQ5#	Resume	3.3V	Native	
GPIO[45]	PCIECLKRQ6#	Resume	3.3V	Native	
GPIO[46]	PCIECLKRQ7#	Resume	3.3V	Native	
GPIO[47]	PEG_A_CLKRQ#	Resume	3.3V	Native	
GPIO[48]	SDATAOUT1	Core	3.3V	GPI	
GPIO[49]	SATA5GP	Core	3.3V	Native	
GPIO[50]	REQ1#	Core	5V	Native	REQ1#
GPIO[51]	GNT1#	Core	3.3V	Native	GNT1#
GPIO[52]	REQ2#	Core	5V	Native	REQ2#
GPIO[53]	GNT2#	Core	3.3V	Native	GNT2#
GPIO[54]	REQ3#	Core	5V	Native	REQ3#
GPIO[55]	GNT3#	Core	3.3V	Native	GNT3#
GPIO[56]	PEG_B_CLKRQ#	Resume	3.3V	Resume	

GPIO[57]	UNMUXED	Resume	3.3V	GPI	
GPIO[58]	SML1CLK	Resume	3.3V	Native	PCH_SML1CLK
GPIO[59]	OC0#	Resume	3.3V	Native	OC0#
GPIO[60]	SML0ALERT#	Resume	3.3V	Native	
GPIO[61]	SUS_STAT#	Resume	3.3V	Native	
GPIO[62]	SUS_CLK	Resume	3.3V	Native	
GPIO[63]	SLP_S5#	Resume	3.3V	Native	SLP_S5#
GPIO[64]	CLKOUTFLEX1	Core	3.3V	Native	
GPIO[65]	CLKOUTFLEX2	Core	3.3V	Native	
GPIO[66]	CLKOUTFLEX2	Core	3.3V	Native	
GPIO[67]	CLKOUTFLEX3	Core	3.3V	Native	CK_48M_SIO
GPIO[72]	UNMUXED	Resume	3.3V	Native	
GPIO[73]	PCIECLKRQ0#	Resume	3.3V	Native	
GPIO[74]	SML1ALERT#	Resume	3.3V	Native	
GPIO[75]	SML1DATA	Resume	3.3V	Native	PCH_SML1DATA

SIO(F71889ED Ver. G)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTNIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

DDR-II DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	00	P/N_DDR0_A P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ#./GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

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History

BOM:

ALL_LED_OFF#要選吃Stand by Power 的pin。

SIO的S5要改接S4(F-71889ED)。

3VSB是否要dual???

R293, R180, R41 要改成0402。

uP6103A要改footprint成有pad的。

北邊那顆PCH Heatsink的rubber要再往南推，以免超過heatsink邊緣。

R11-2491T13-K14要從AVL移除，

R134要上件，且VTT_Enable改pull CPU_VTT。

3VSB_WAKE#的Vcontroll要接ATX_5VSB。

SVDIMM_IN的二顆470uf，6.3V的電容要上。

uP6213要針對green choke和offset做fine tune。

CPU背面的0603要換X7R。

SLP_LAN# PULL HI。

生產加工注意事項加測5VDRV1。

C108多並一顆0.1uf (C134) Power Team suggest for Green CHOKE。

Mouse要接到pinheader的pin4和pin5。

PLTRST#要加一顆100ohm的dampning電阻。

USB disable Port6, Port7。

USB mode要選吃Stand by Power 的pin。

GPIO33要留jump。

全部不要用green choke。

EUP Solution.

clear CMOS, patch 線路。

alc889, co-lay。

HDMI 5V要不要用MOS切???

PCI CLK 線長。

R599要上件。

C655改成10nf。

GPU超壓換R851換61.9 OHM。

CLKRQ B to gnd。

hi low side MOS修改avl。

PCB Layout:

DDR加壓。

www.aitech1.ru

加power team solution:

R979 = 22K ohm.

CPU Vcore和CPU_VTT output CHOKE都re-work成0.5u的CHOKE，

R709 = 3K ohm.

C636 = 33pf.

C108多並一顆0402電容的pad，(if use green CHOKE, then Cap 用0.1uf)

R59 = 180 K ohm.

R757 = 14K ohm.

R124 = 22K ohm.

R38 = 47K ohm.

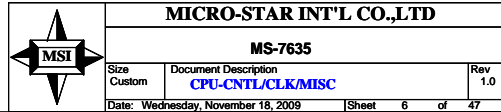
R285 = R190 = R331 = 100K ohm.

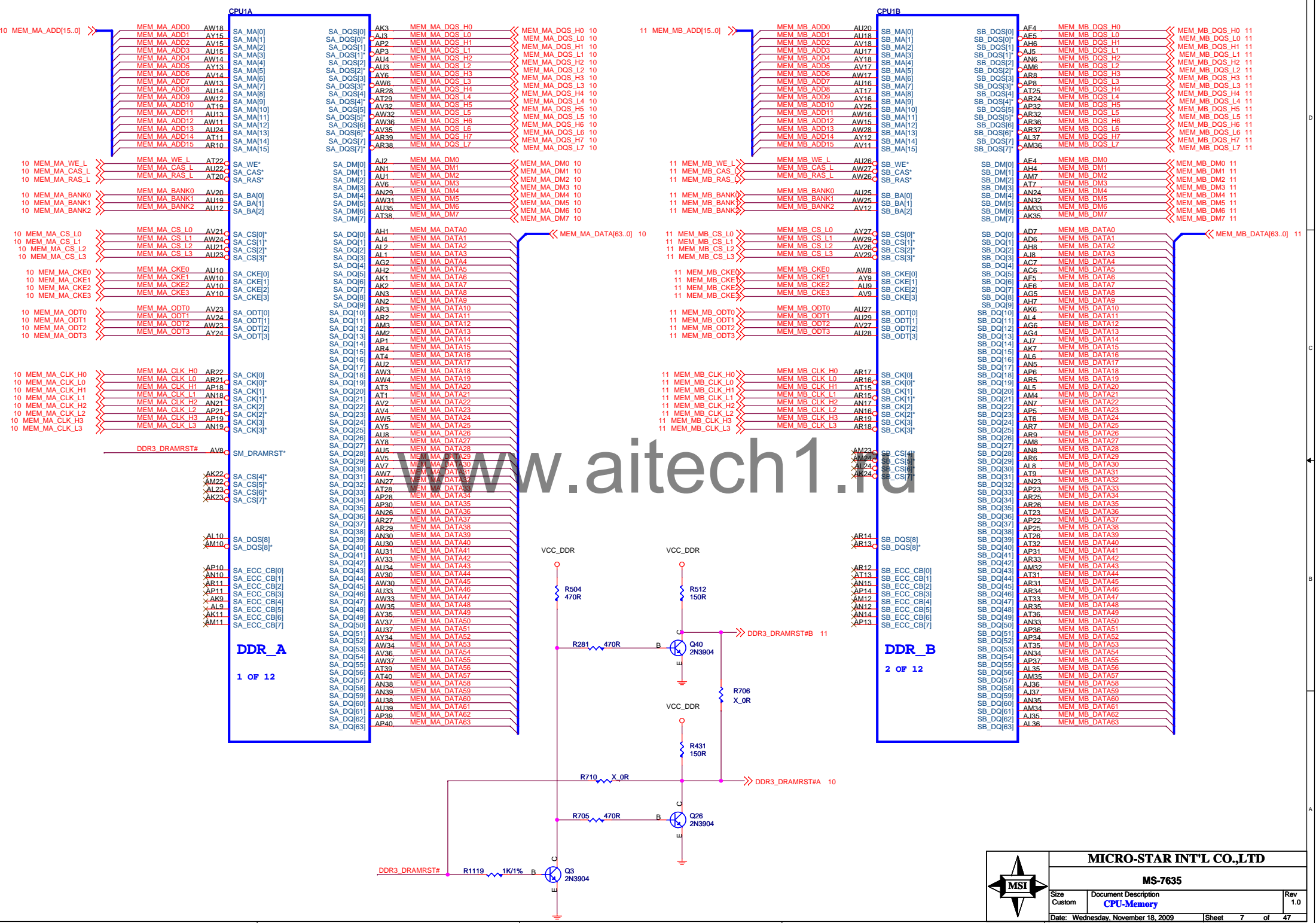


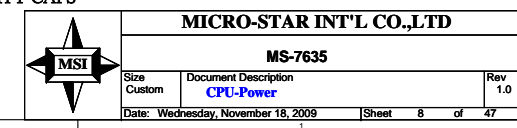
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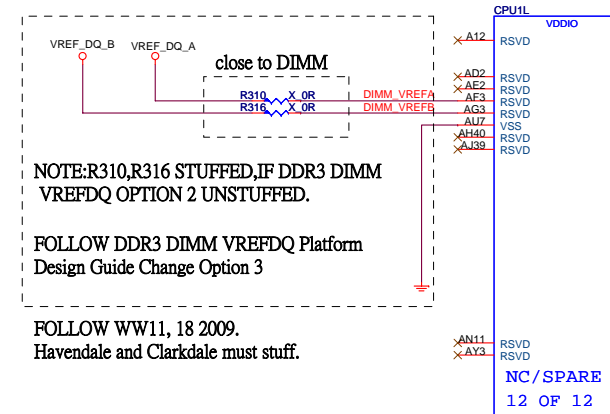
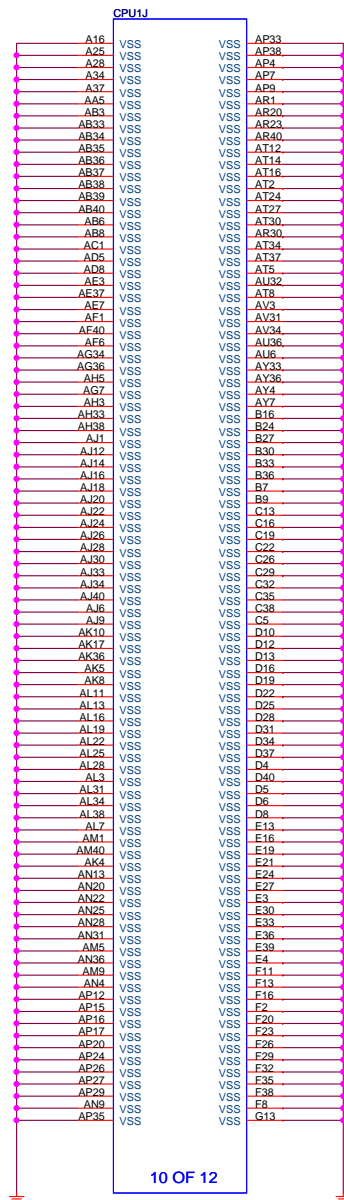
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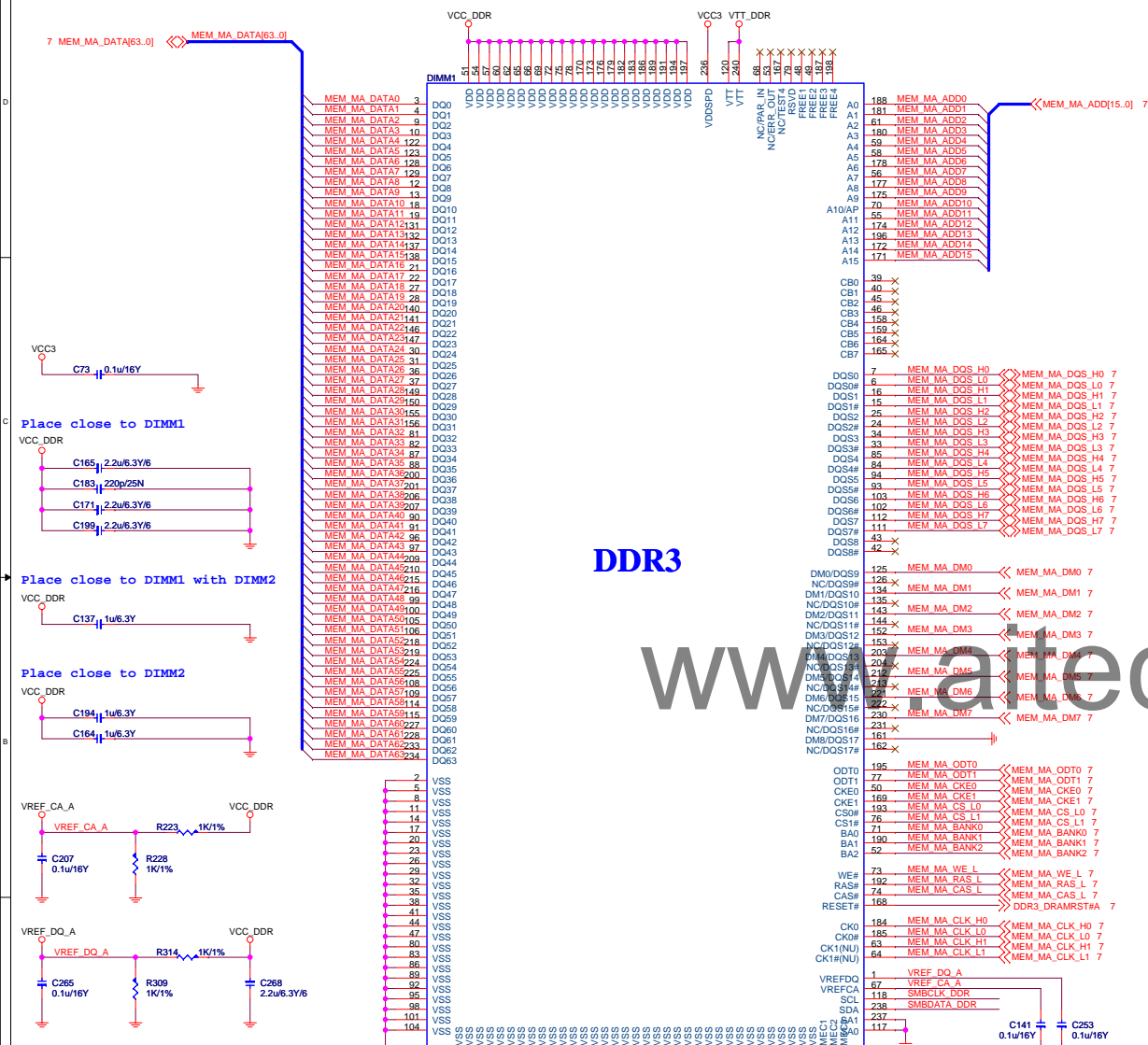




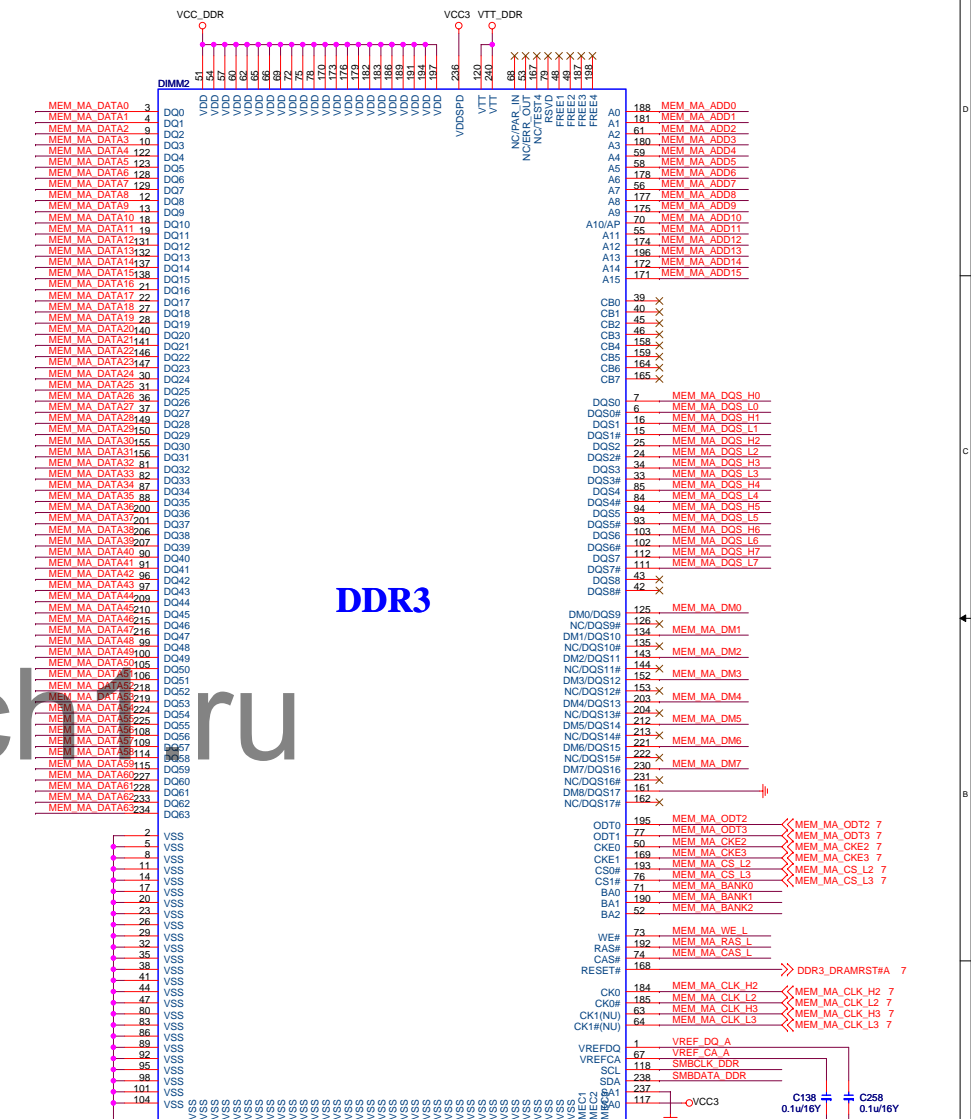


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DDRIII DIMM_A1

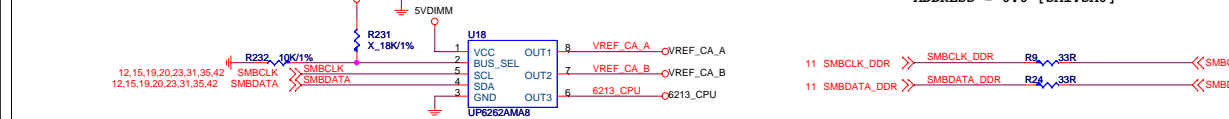


DDRIII DIMM_A2



UPI VOLTAGE CONSOLE

0x6A: RH=OPEN, RL=10K



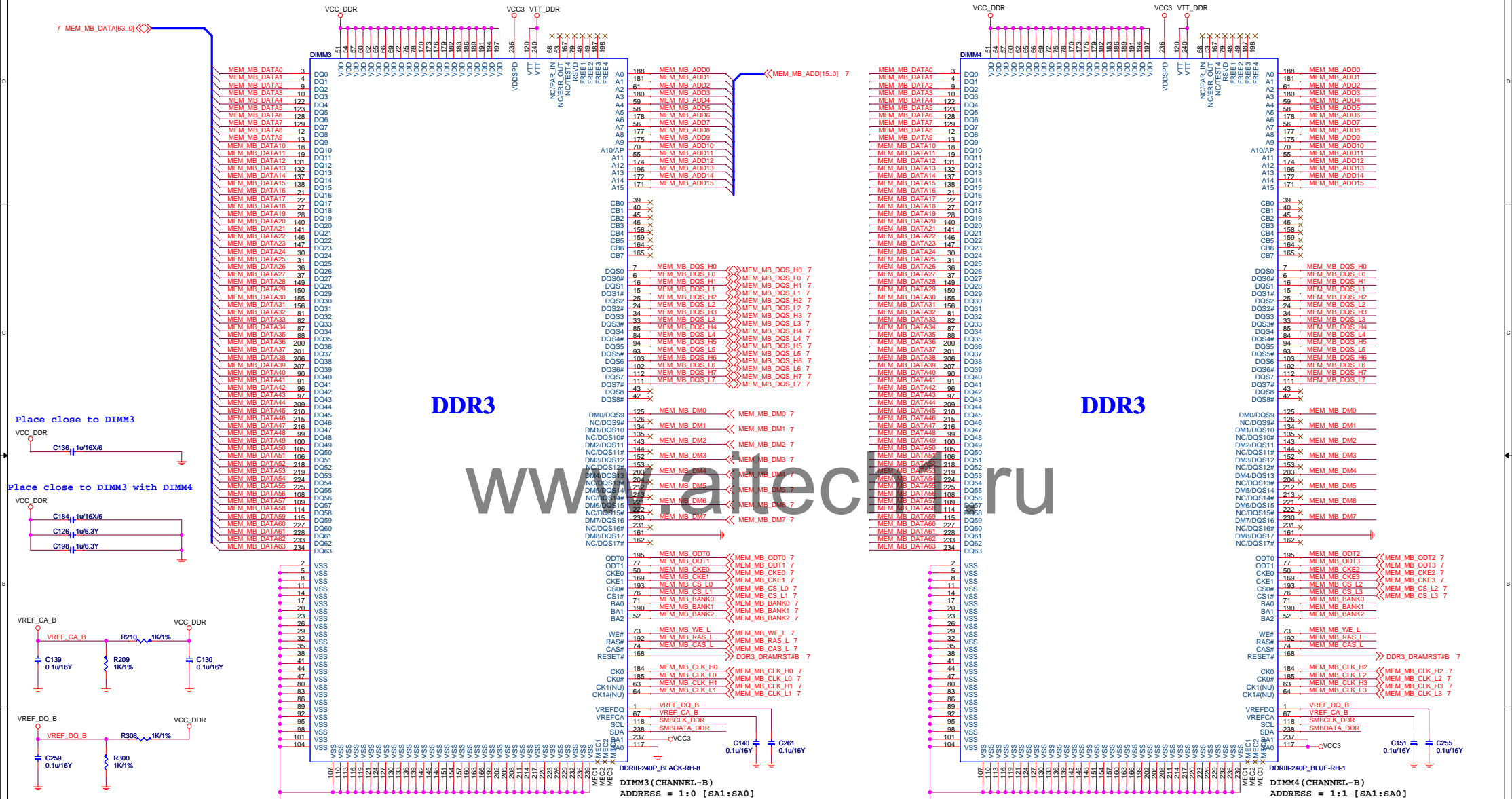
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DDR3 DIMM_B1

DDR3 DIMM_B2



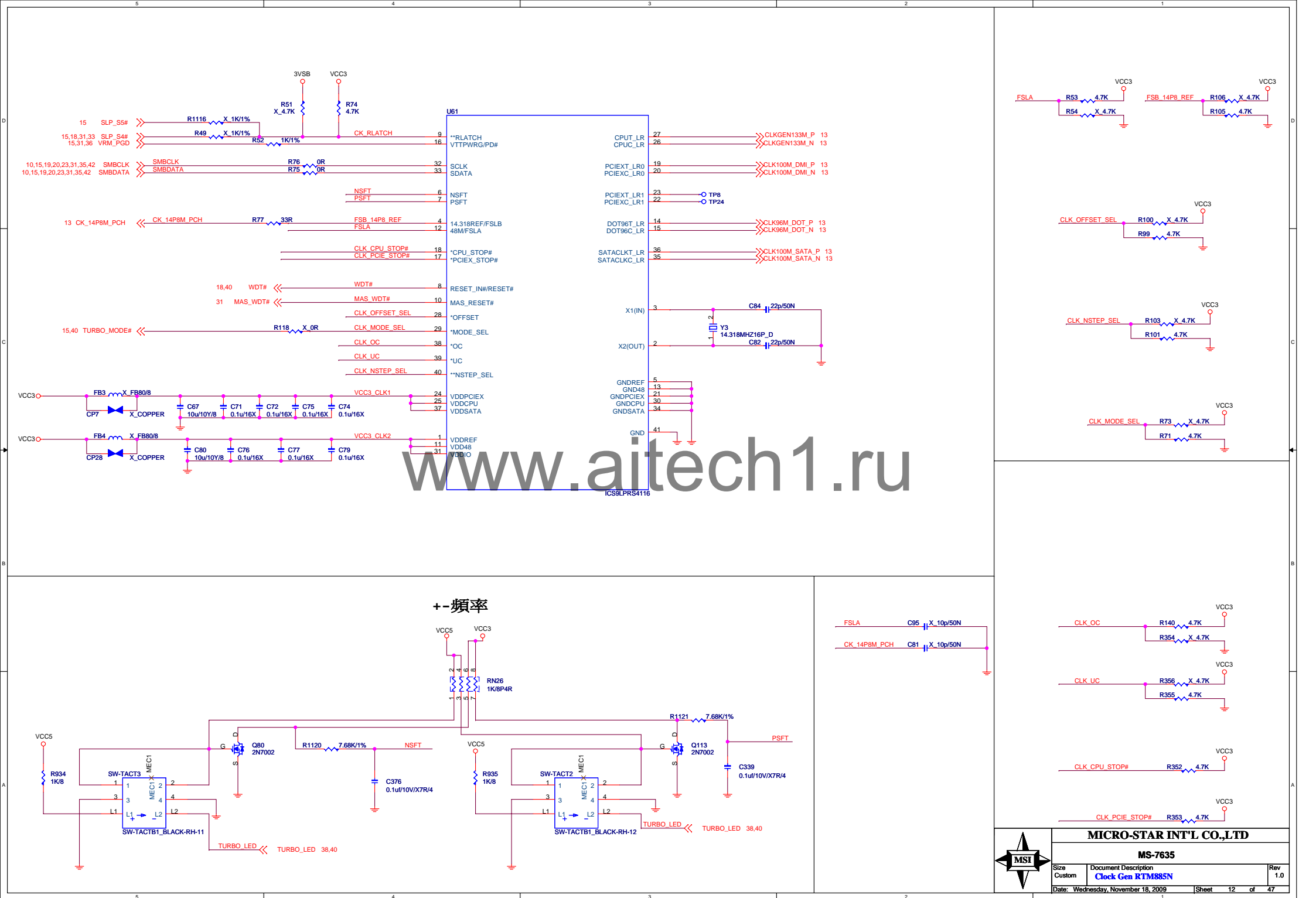
Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

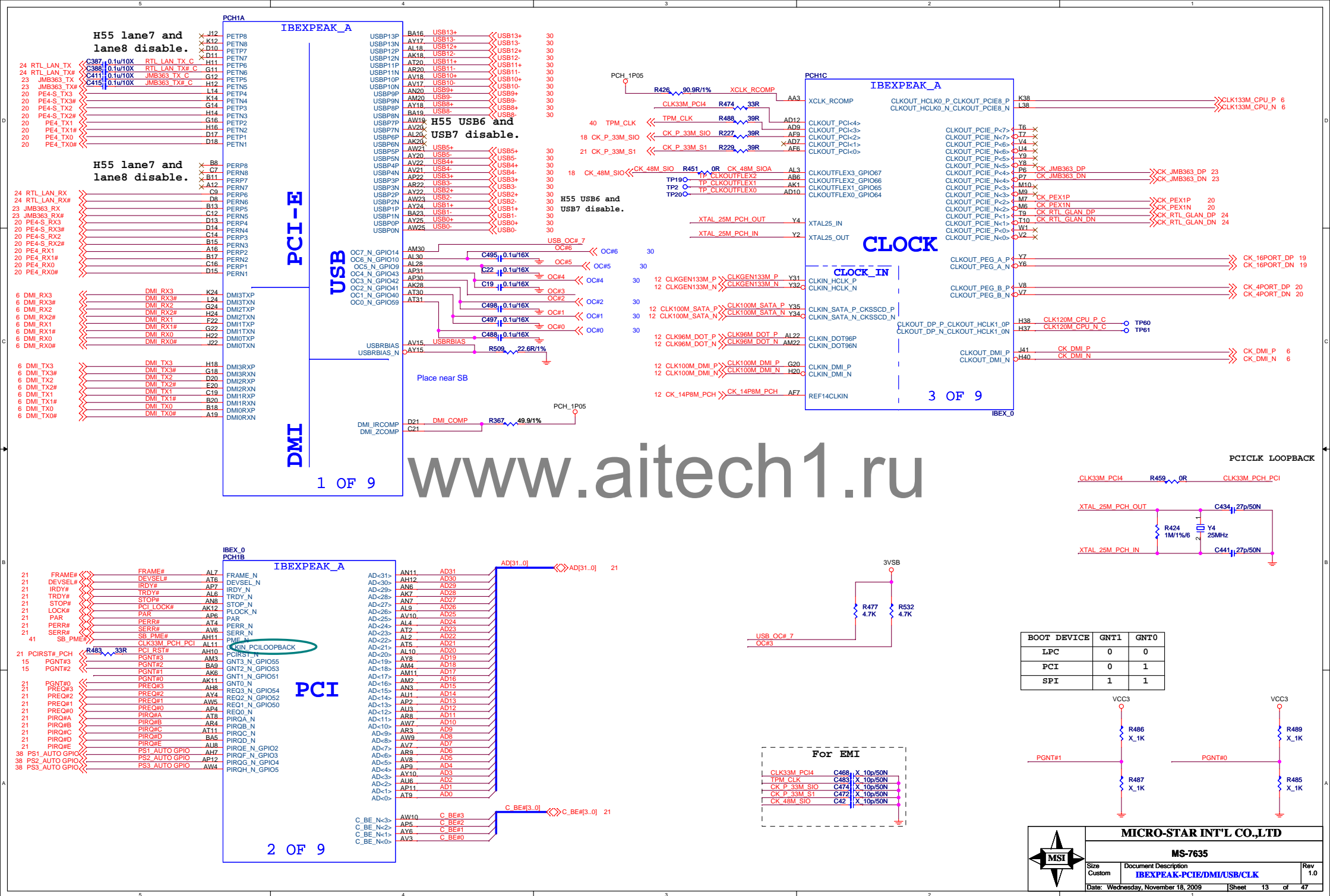
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

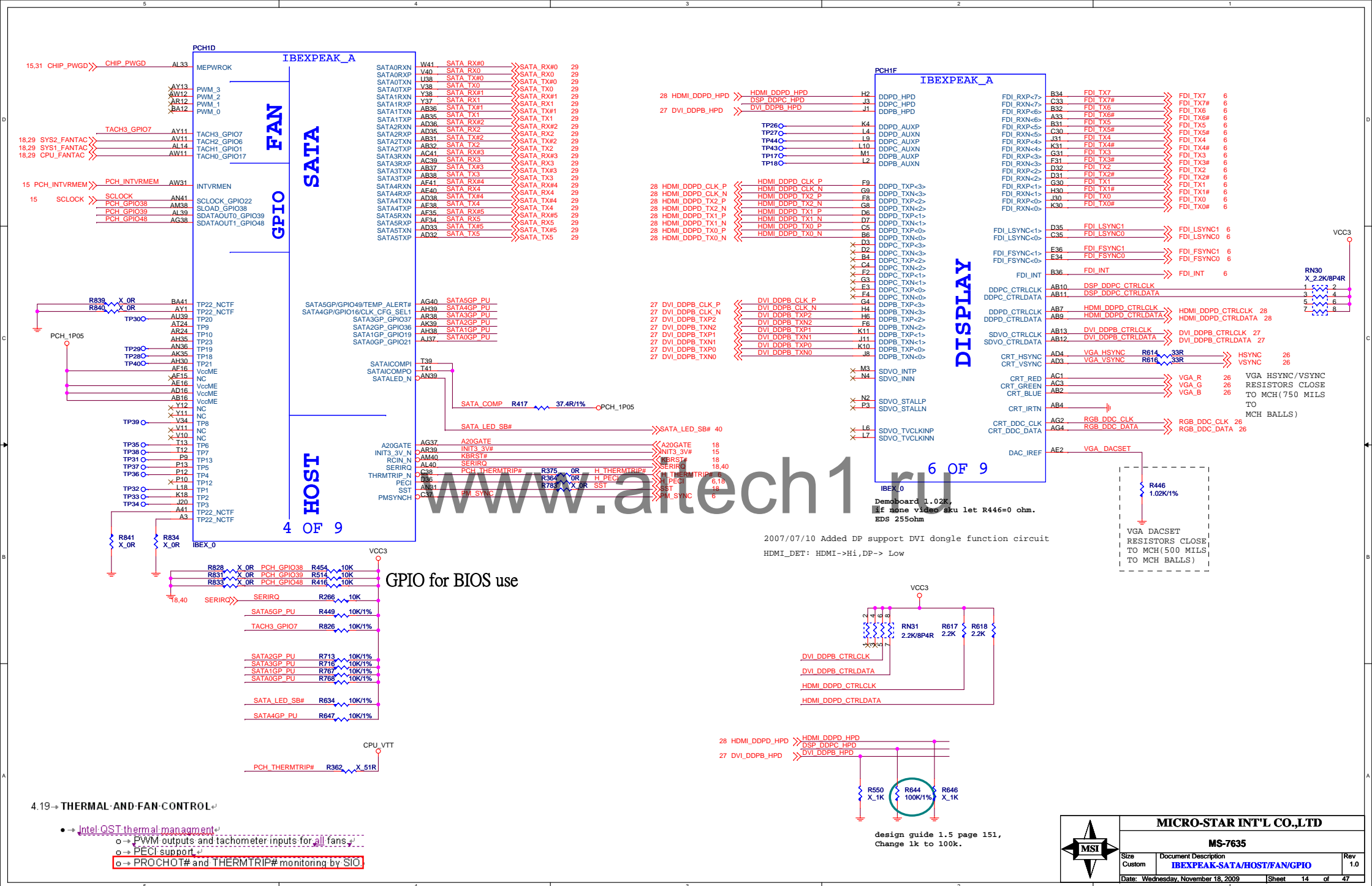
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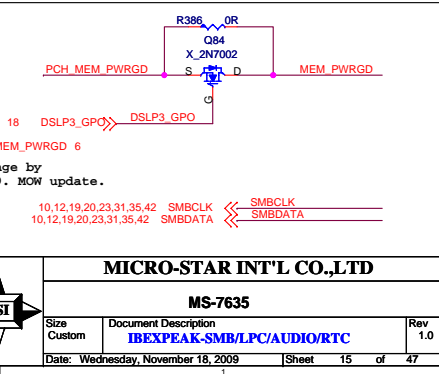
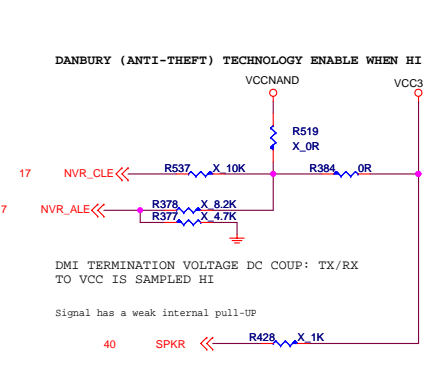
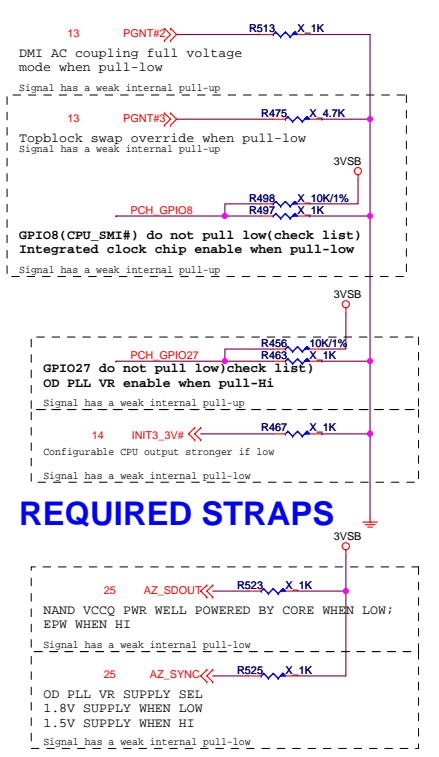
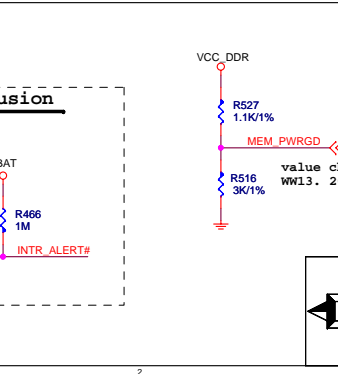
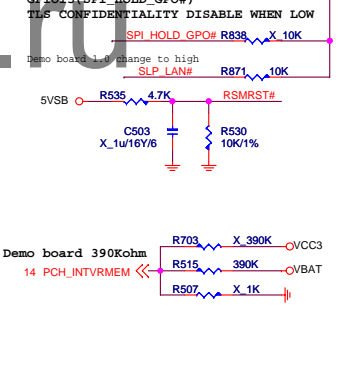
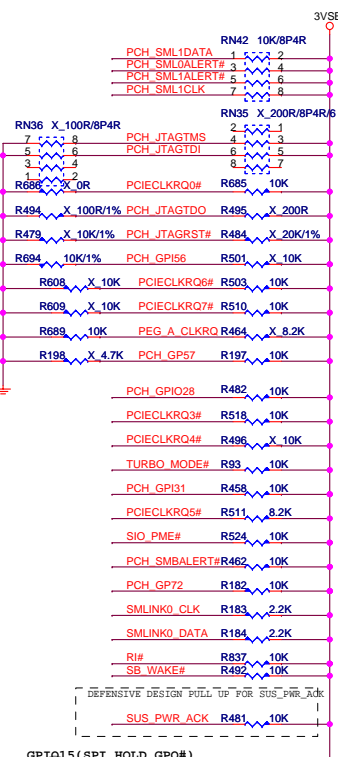
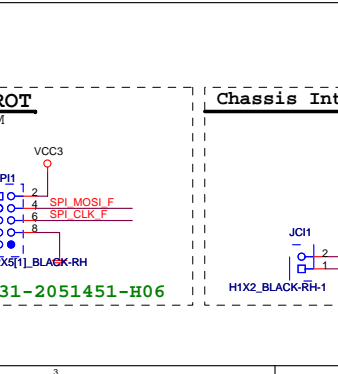
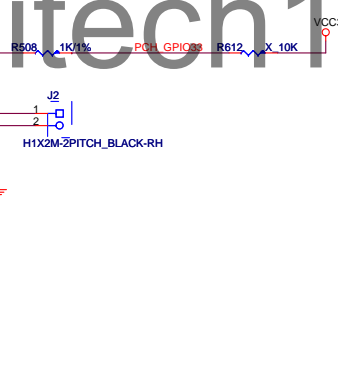
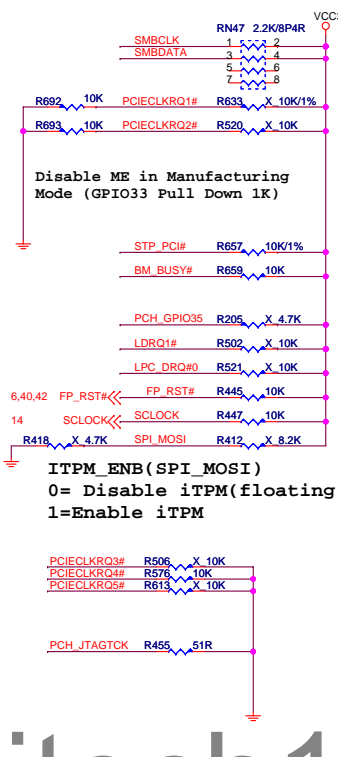
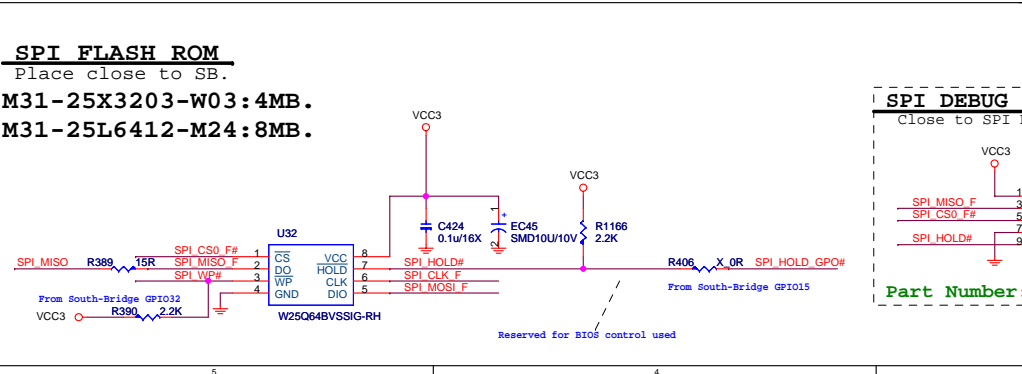
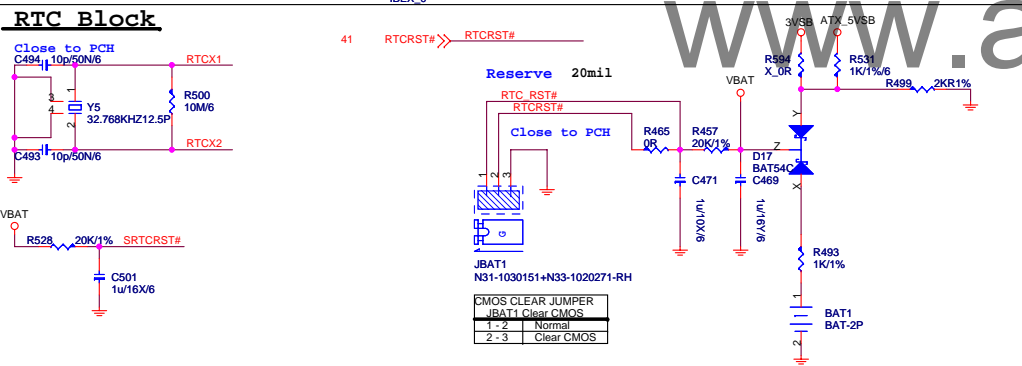
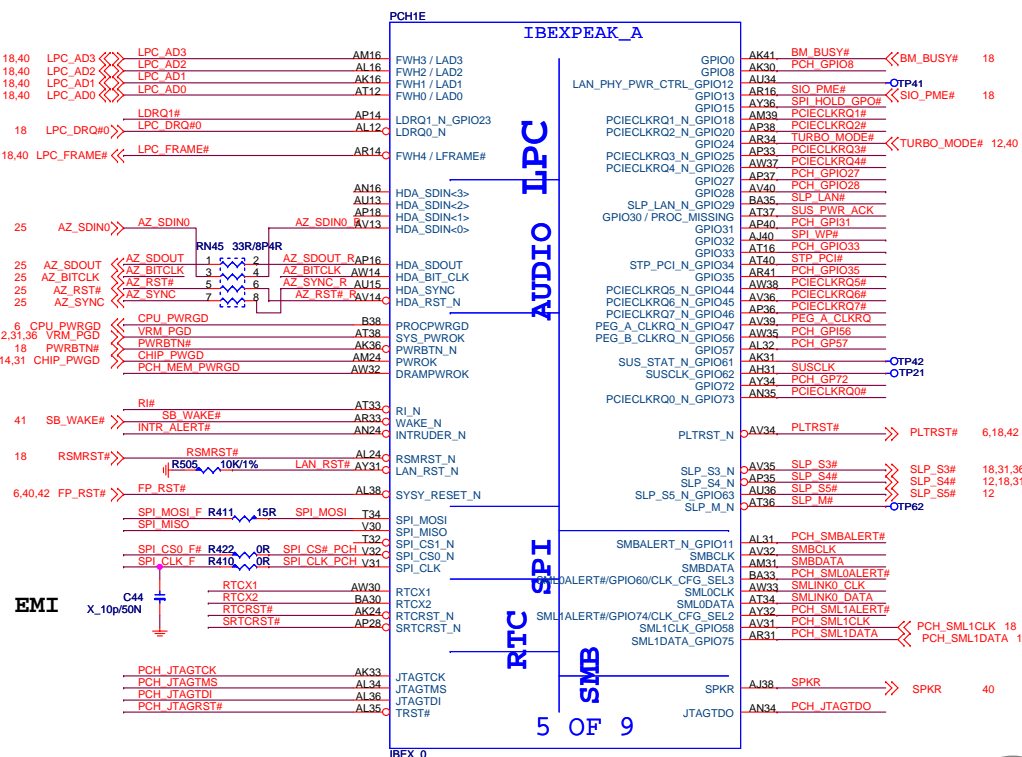
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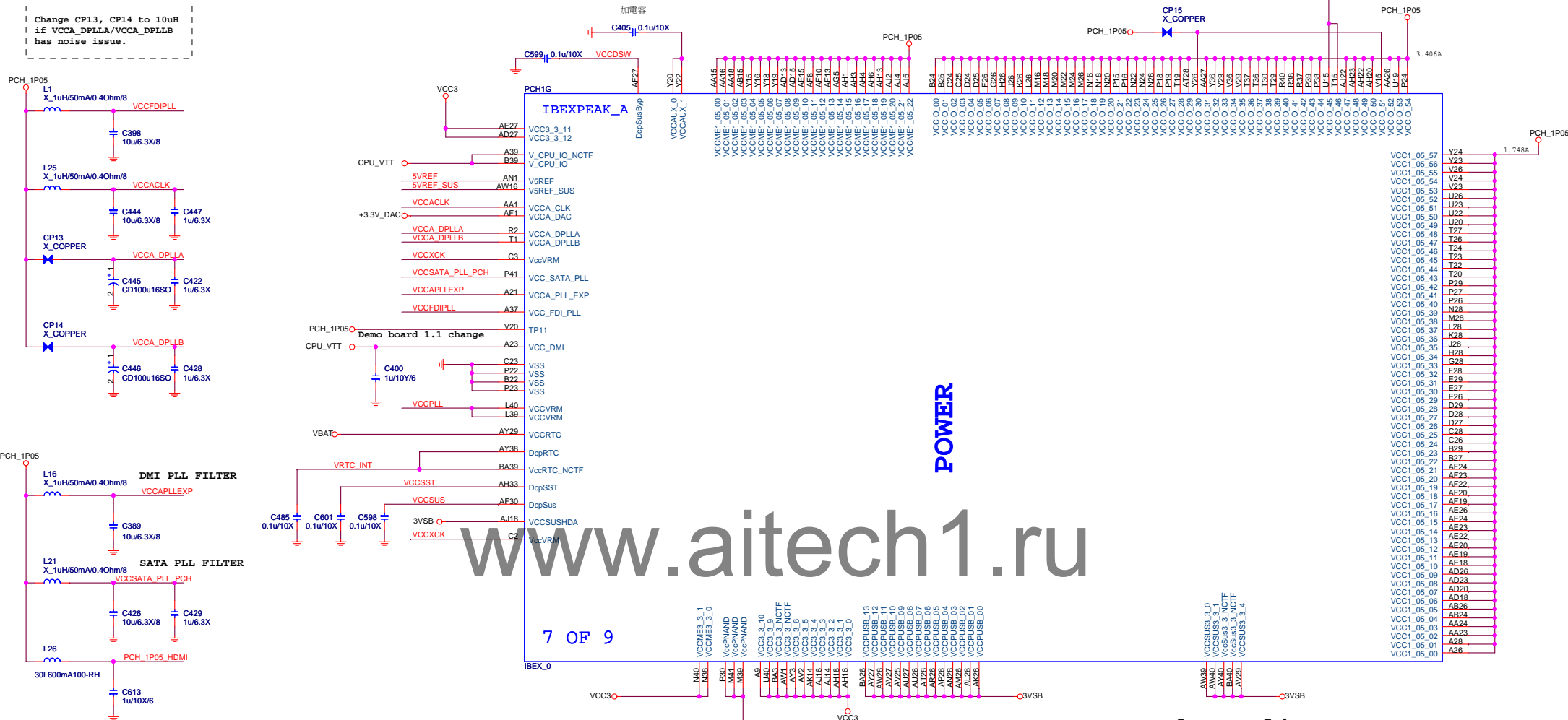
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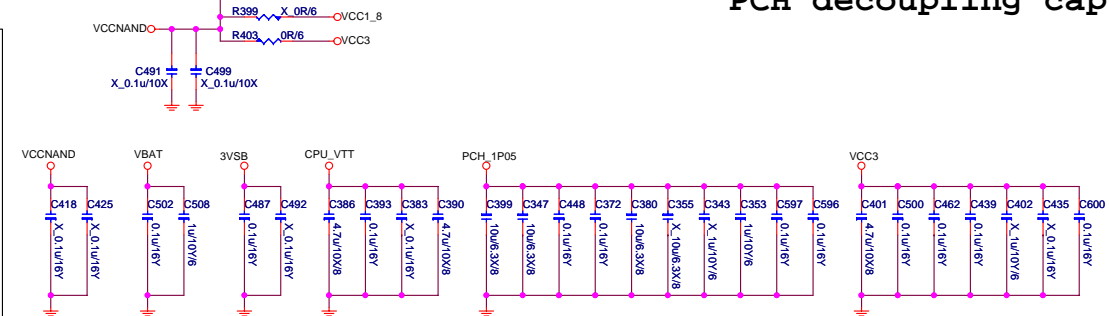
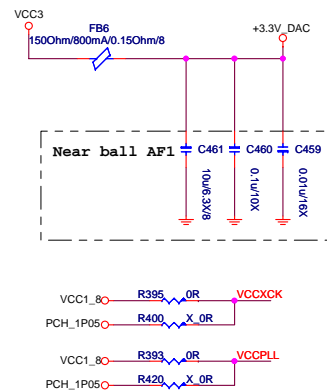
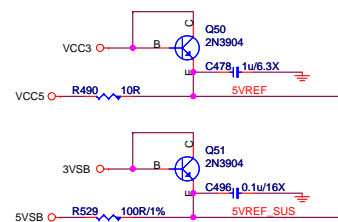


```
| Change CP13, CP14 to 10uH
| if VCCA_DPLLA/VCCA_DPLLB
| has noise issue.
```



5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



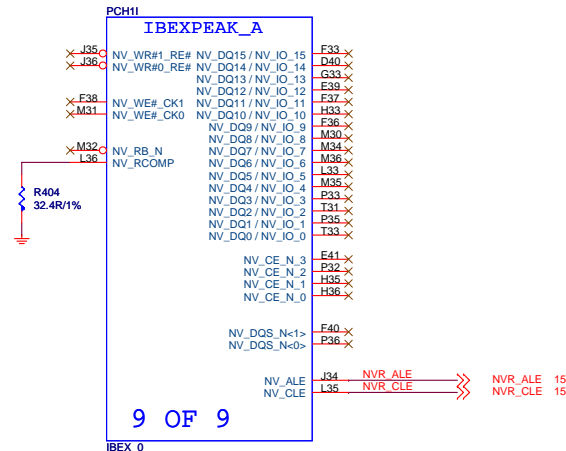
PCH decoupling cap

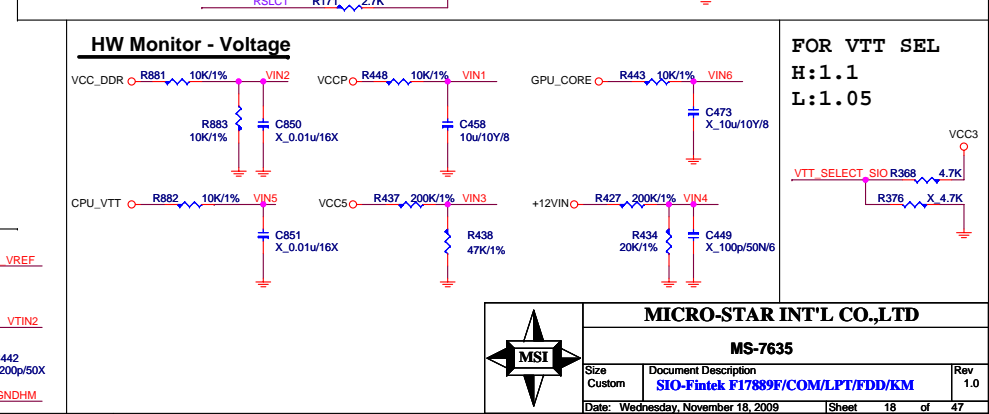
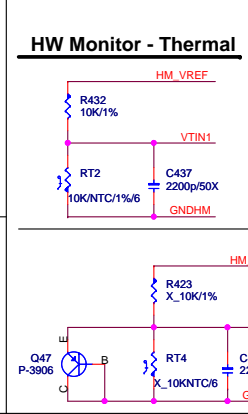
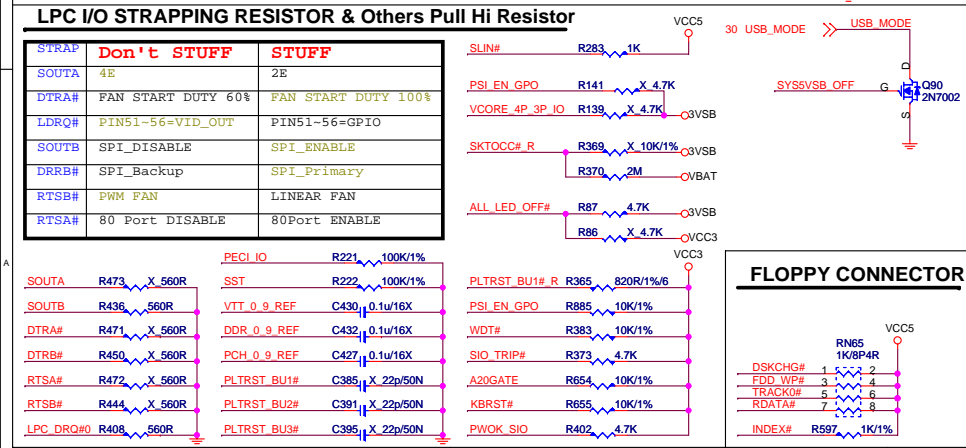
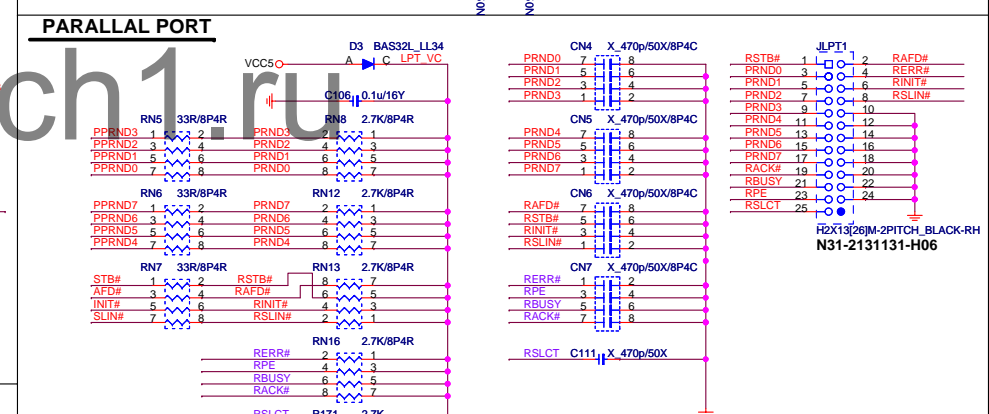
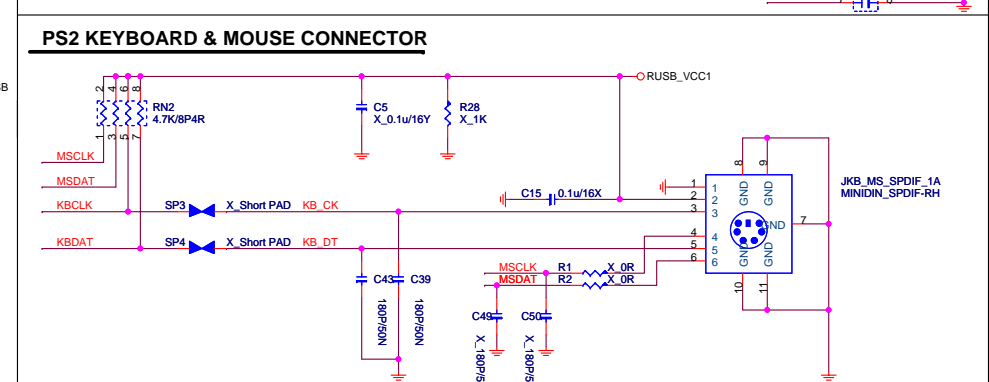
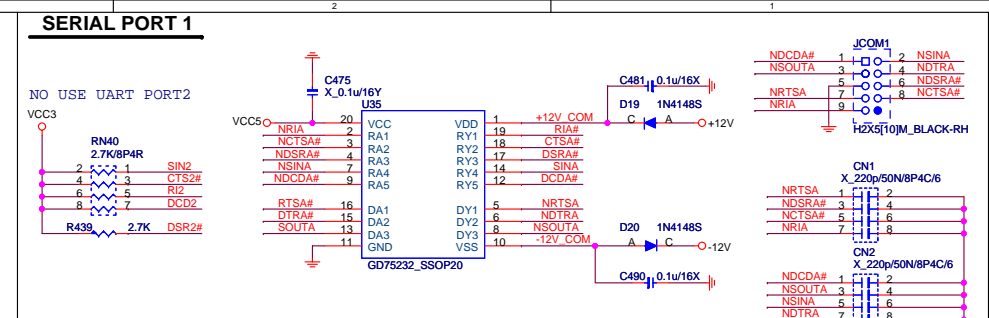
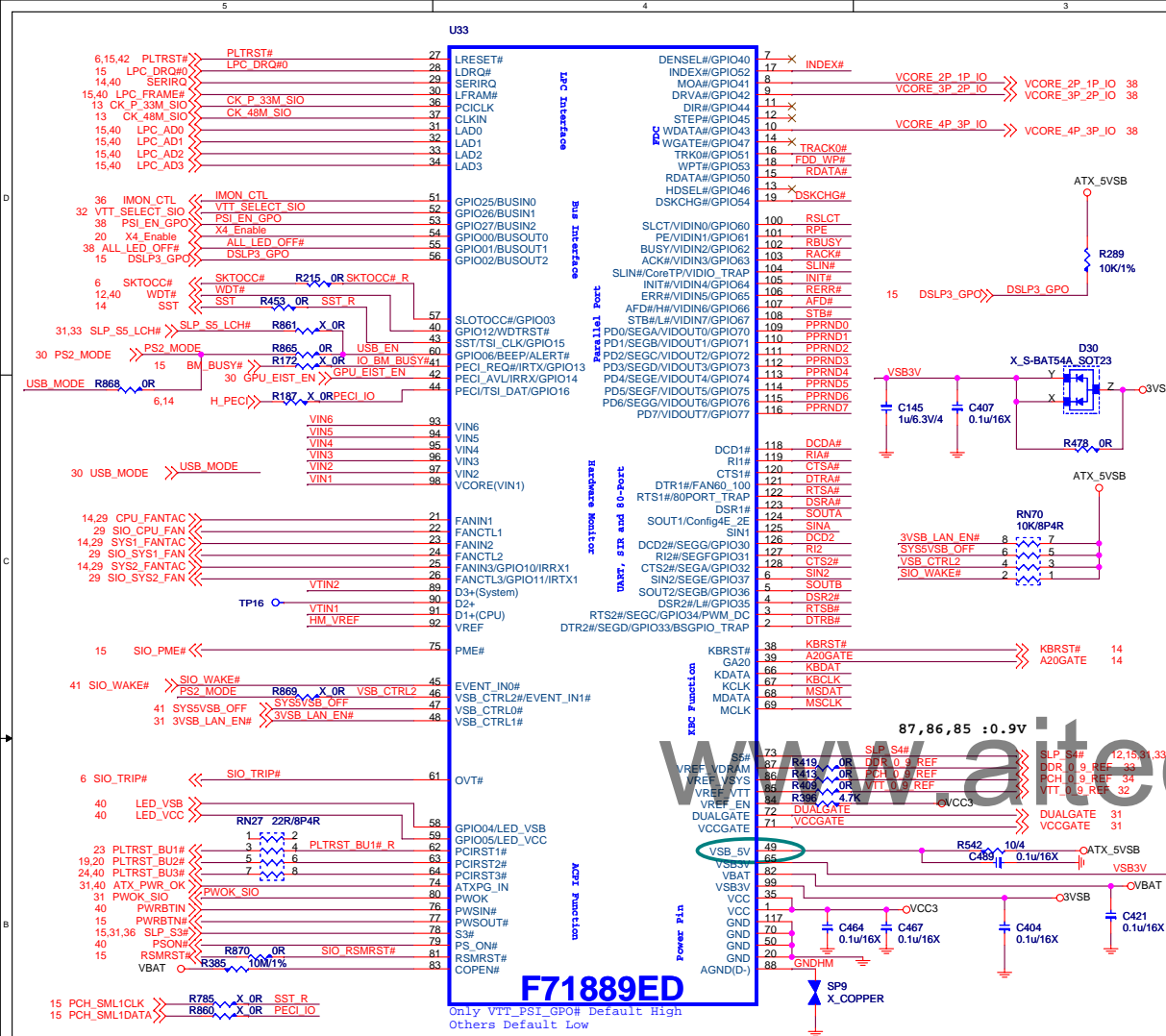


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description IBEXPEAK-POWER	Rev 1.0
Date: Wednesday, November 18, 2009		Sheet 16 of 47





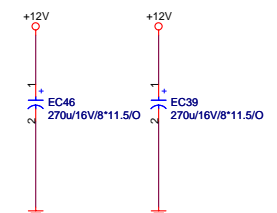
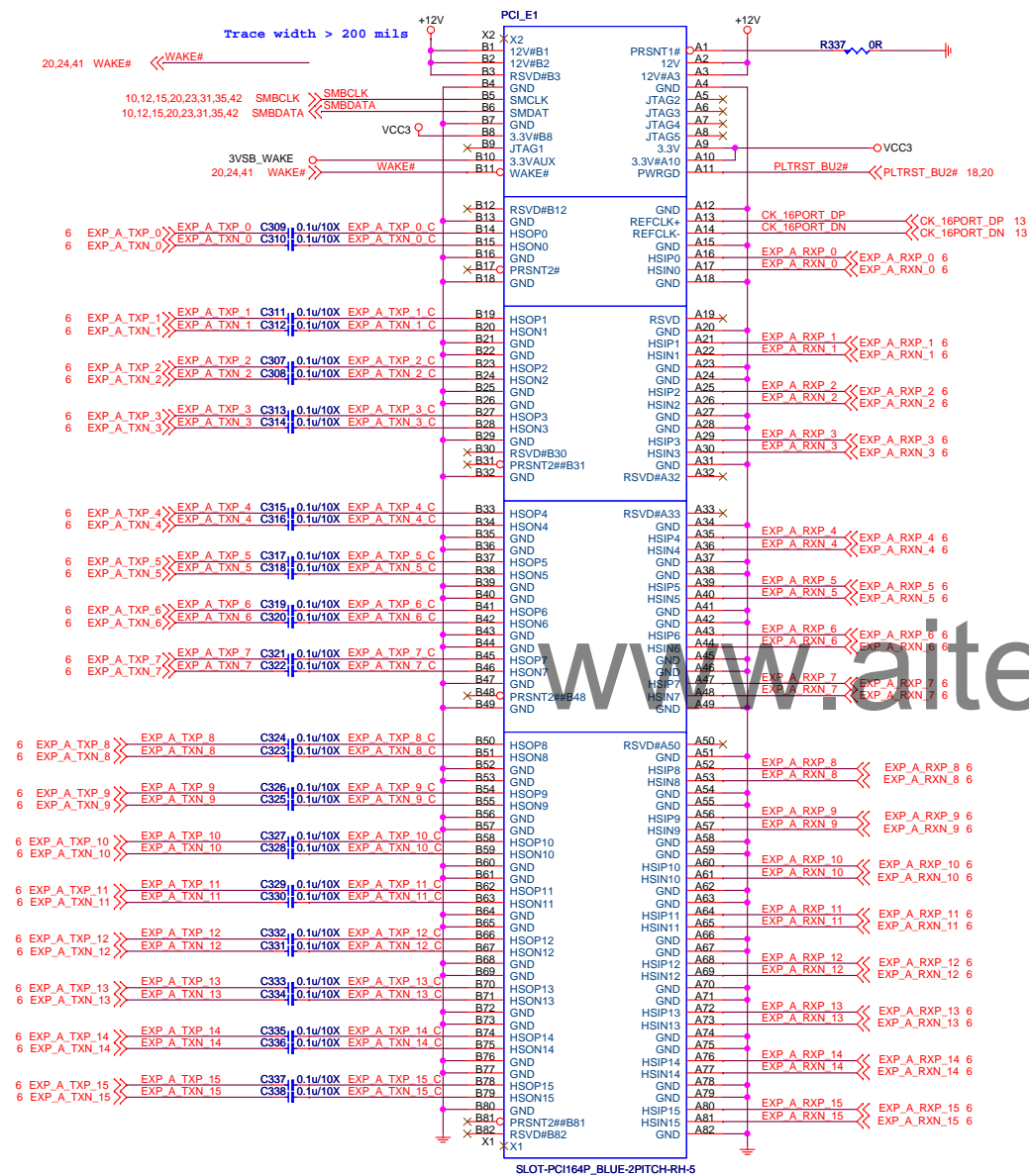
MICRO-STAR INT'L CO.,LTD

MS-7635

Size Custom Document Description **SIO-Fintek F71889F/COM/LPT/FDD/KM** Rev 1.0

Date: Wednesday, November 18, 2009 Sheet 18 of 47

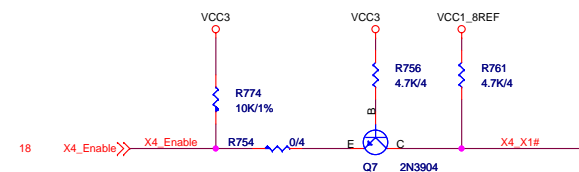
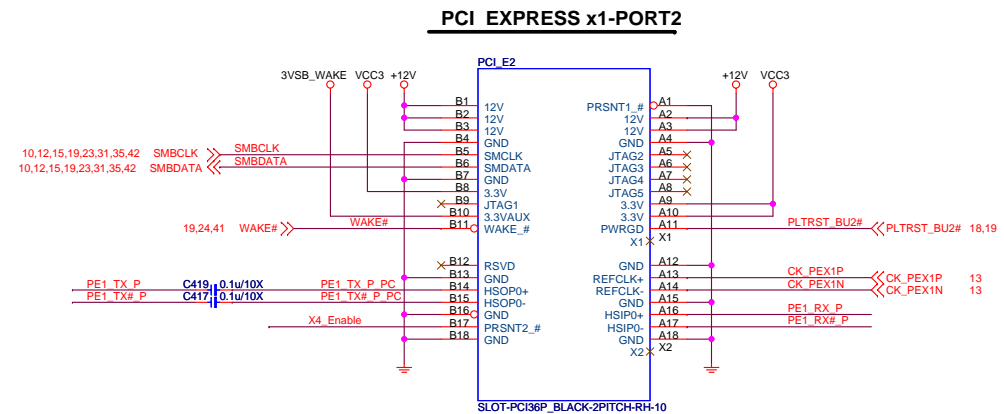
PCI_Express X16 slot



MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description PCIE x16 Slot	Rev 1.0
Date: Wednesday, November 18, 2009		Sheet 19 of 47

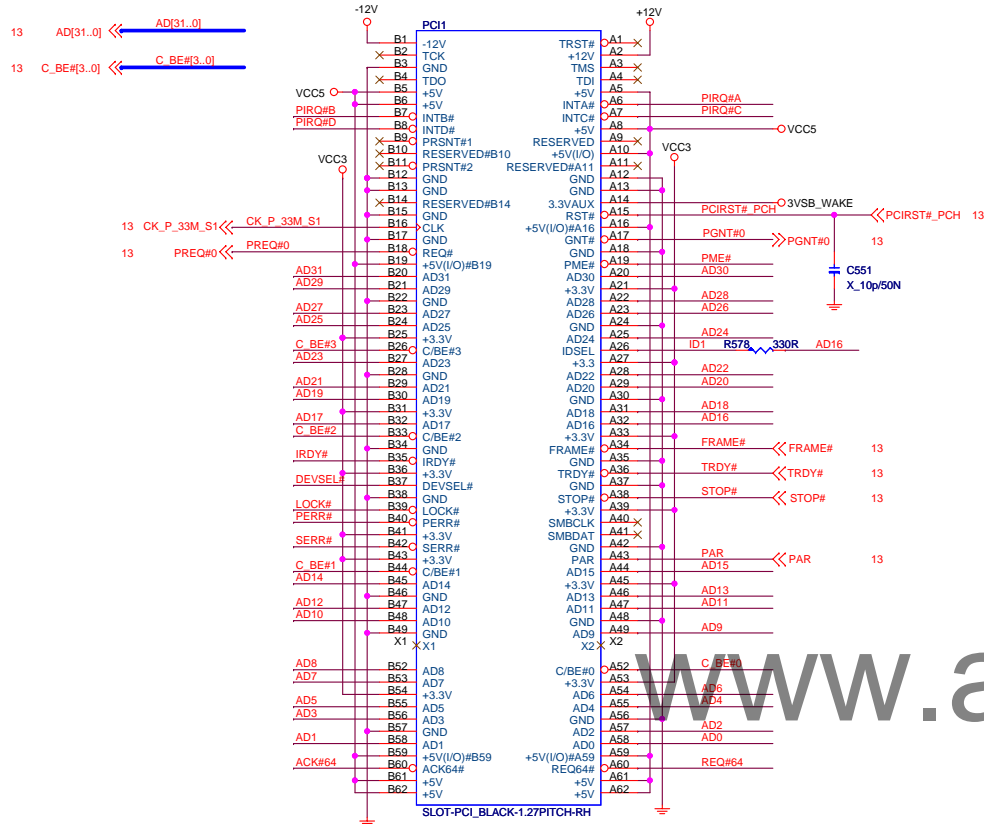


SEL (X4 Slot_Enable)	Output	PCI-E_Slo
Hi	B2	X4 / X0
Low	B1	X2 / X1



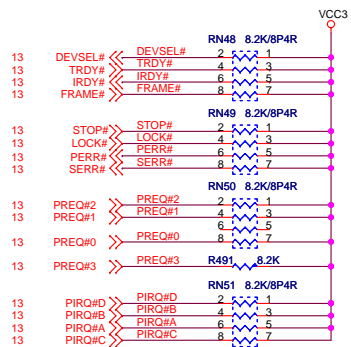
Size Custom	Document Description X4 / X1 SWITCH	Rev 1.0
Date: Wednesday, November 18, 2009		Sheet 20 of 47

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

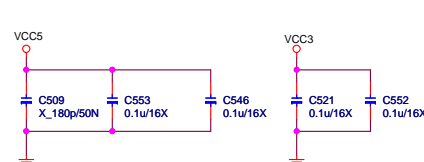


ISDEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



VT6308P - 1394 暫時先移除此SPEC.

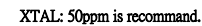
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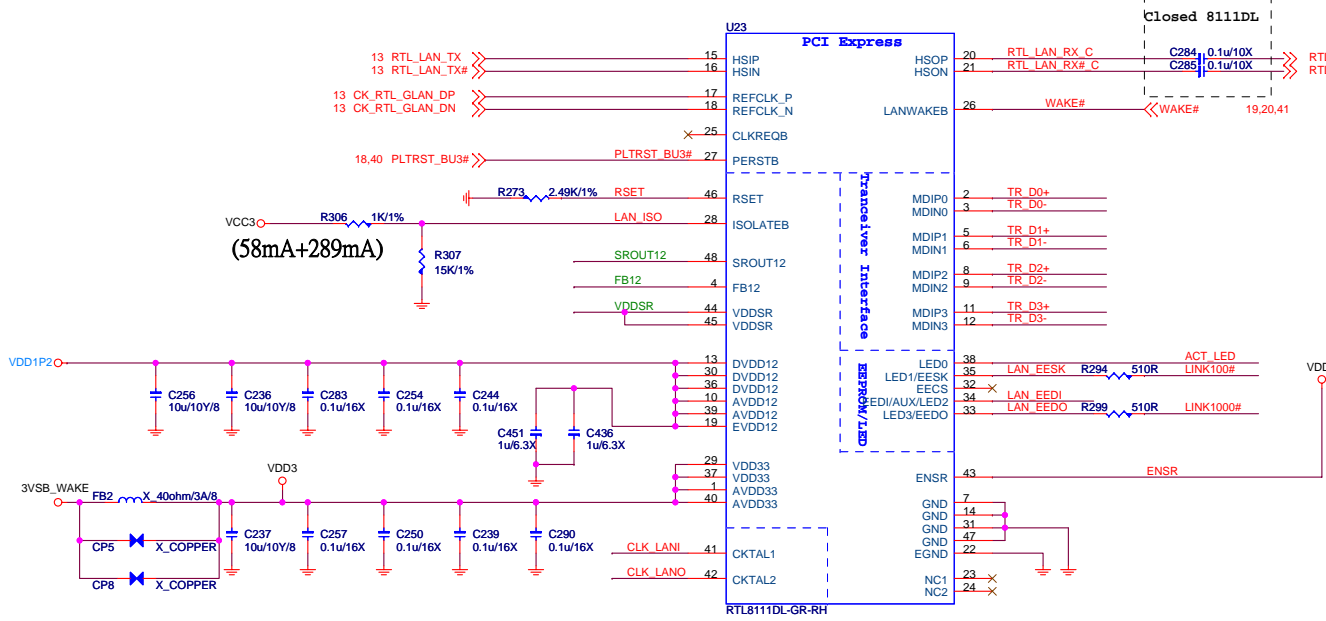


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description 1394 Controller - VT6308P	Rev 1.0
Date: Tuesday, November 17, 2009		
Sheet 22 of 47		





Closed 8111DL

C284 0.1u/10X
C285 0.1u/10X

WAKE# 19,20,41

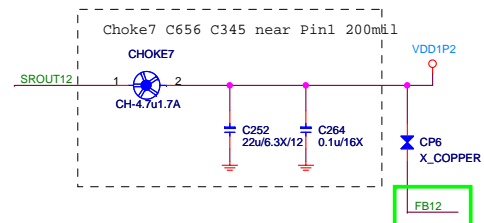
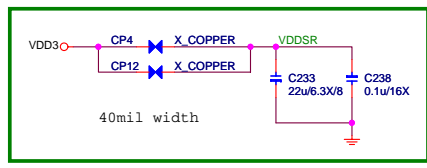
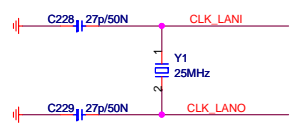
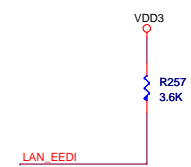
TR_D0+
TR_D0-
TR_D1+
TR_D1-
TR_D2+
TR_D2-
TR_D3+
TR_D3-

ACT_LED
LINK100#
LAN_EESK R284 510R
LAN_EEDI R299 510R
LINK1000#

ENSR

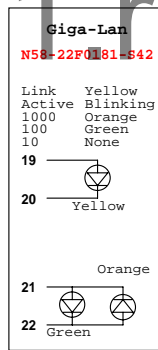
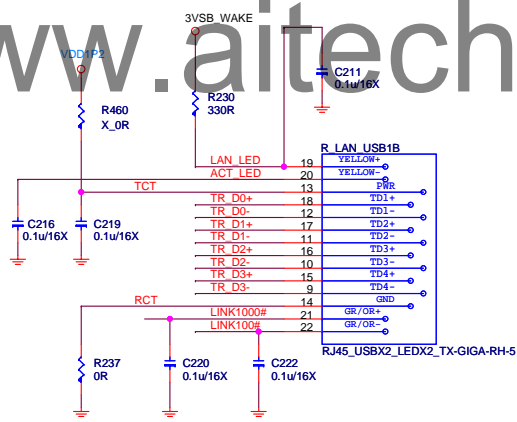
GND
GND
GND
GND
ENGND

NC1
NC2



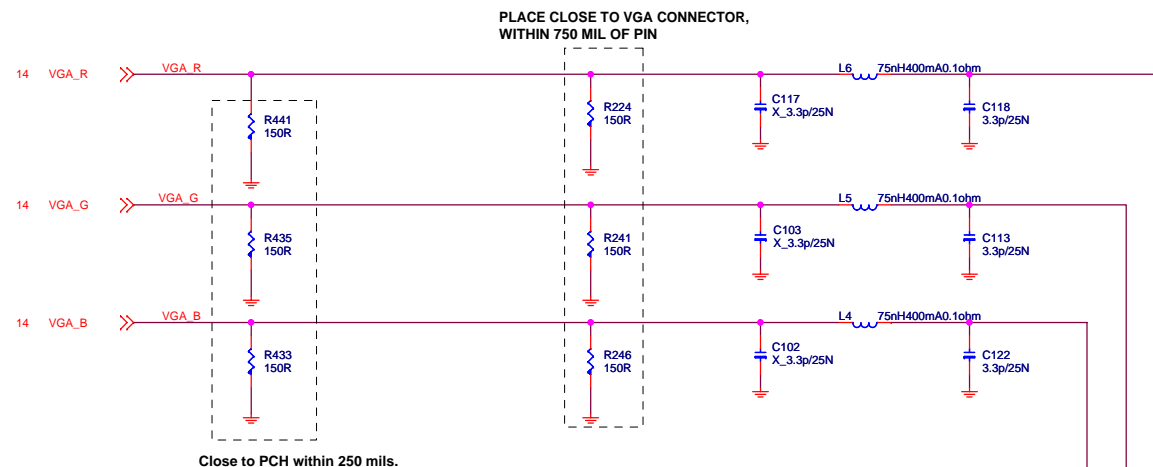
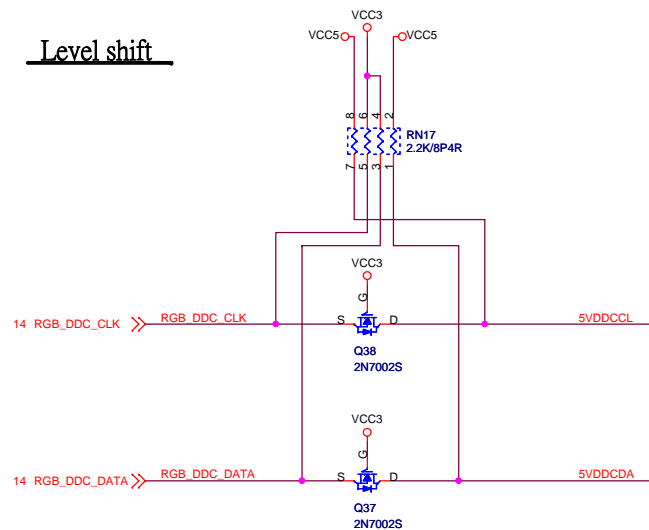
"FB12": A trace front CHOKE to RTL8111DL pin5

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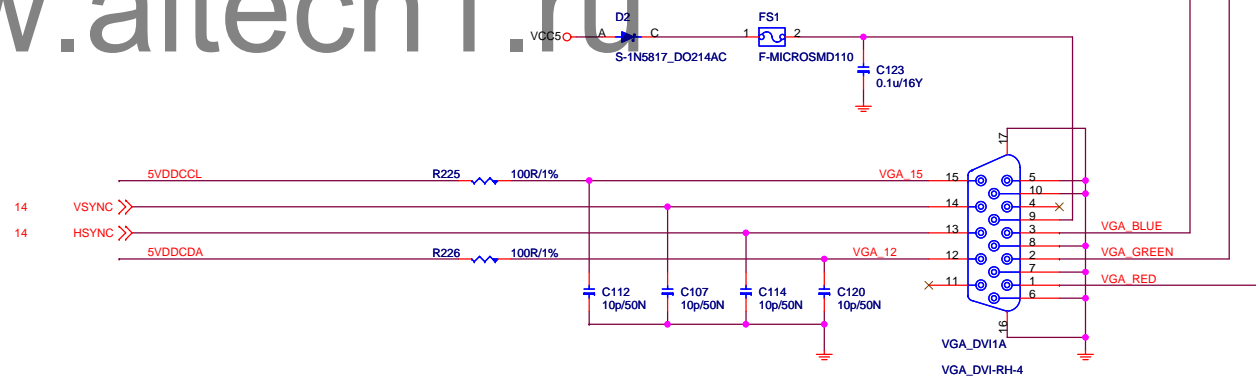
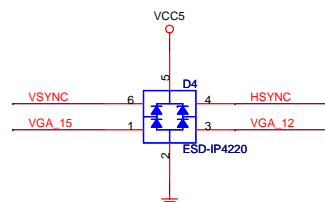
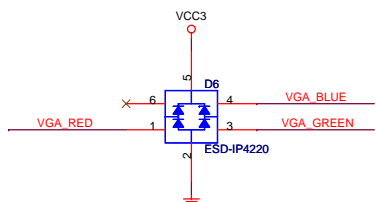


D-Sub

Level shift



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MICRO-STAR INT'L CO.,LTD

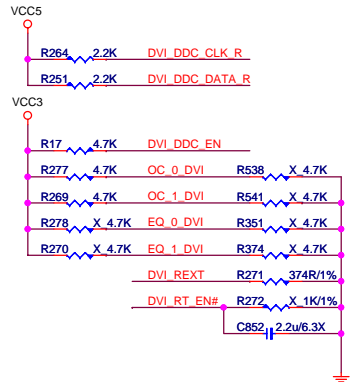
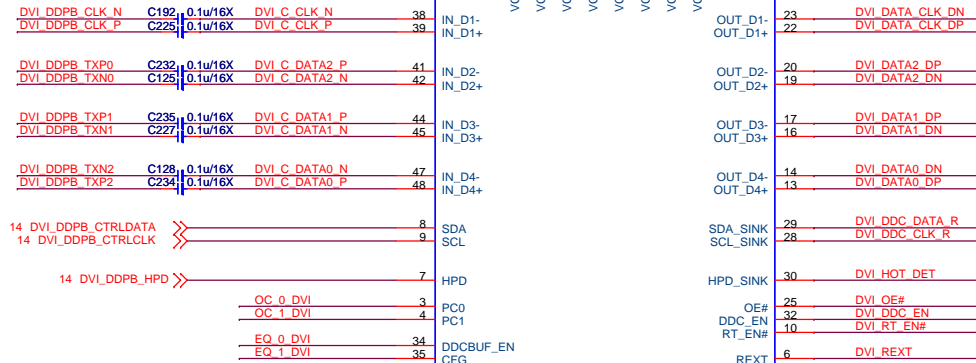
MS-7635

Size	Document Description	Rev
Custom	VGA	1.0

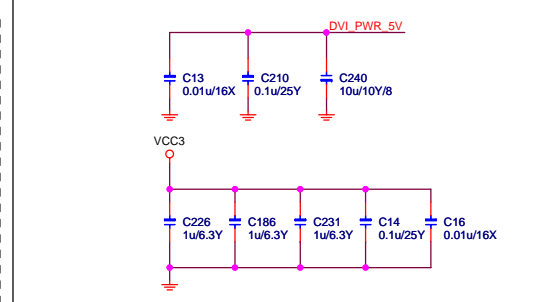
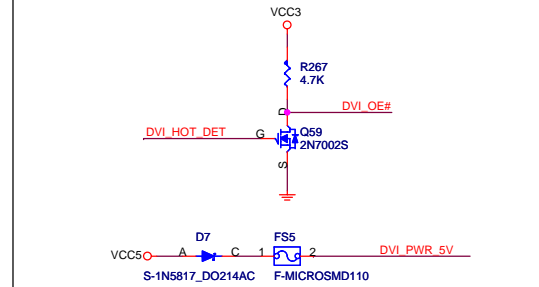
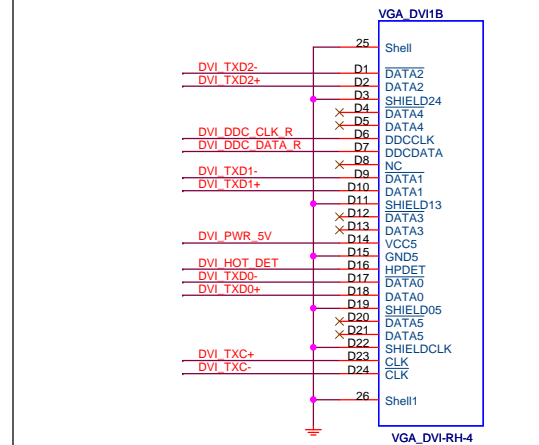
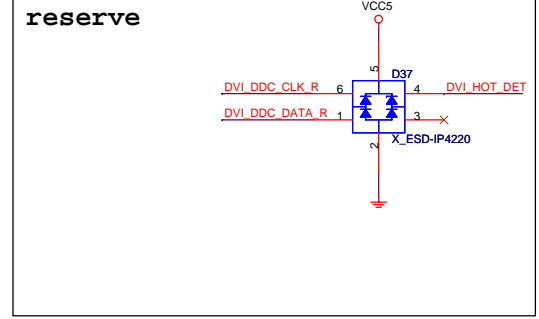
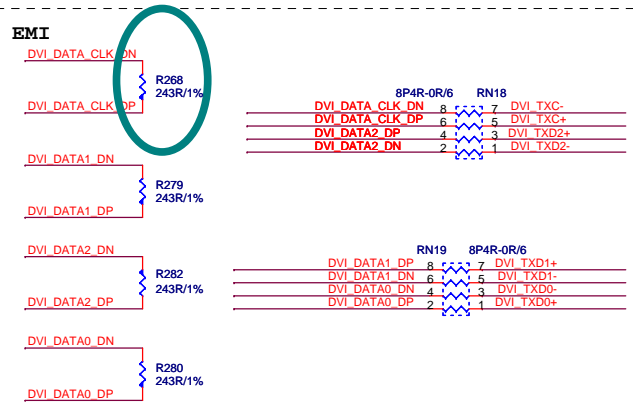
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DVI level shifter

14 DVI_DDPB_TXP0
14 DVI_DDPB_TXN0
14 DVI_DDPB_TXP1
14 DVI_DDPB_TXN1
14 DVI_DDPB_TXP2
14 DVI_DDPB_TXN2
14 DVI_DDPB_CLK_P
14 DVI_DDPB_CLK_N

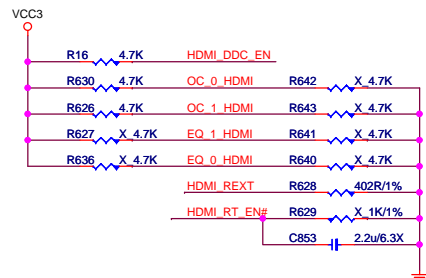
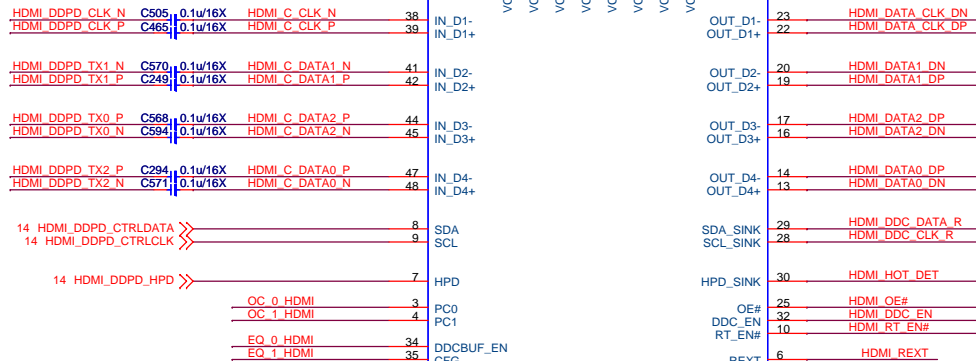


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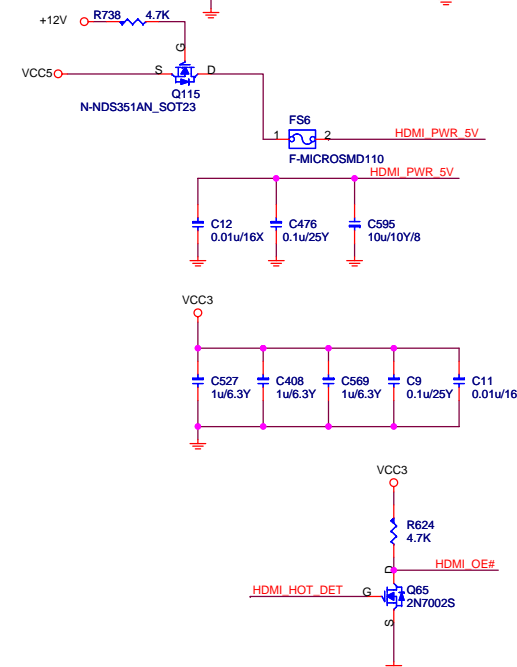
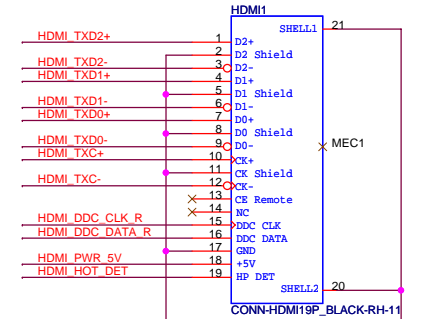
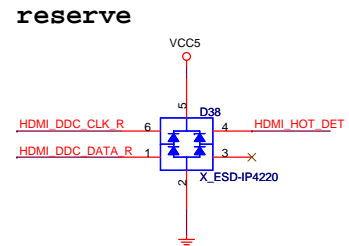
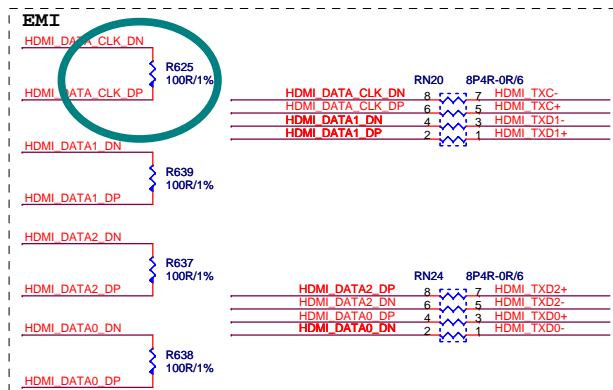
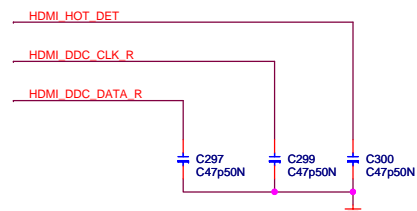


HDMI level shifter

14 HDMI_DDPD_CLK_P <<< HDMI_DDPD_CLK_P
14 HDMI_DDPD_CLK_N <<< HDMI_DDPD_CLK_N
14 HDMI_DDPD_TX2_P <<< HDMI_DDPD_TX2_P
14 HDMI_DDPD_TX2_N <<< HDMI_DDPD_TX2_N
14 HDMI_DDPD_TX1_P <<< HDMI_DDPD_TX1_P
14 HDMI_DDPD_TX1_N <<< HDMI_DDPD_TX1_N
14 HDMI_DDPD_TX0_P <<< HDMI_DDPD_TX0_P
14 HDMI_DDPD_TX0_N <<< HDMI_DDPD_TX0_N



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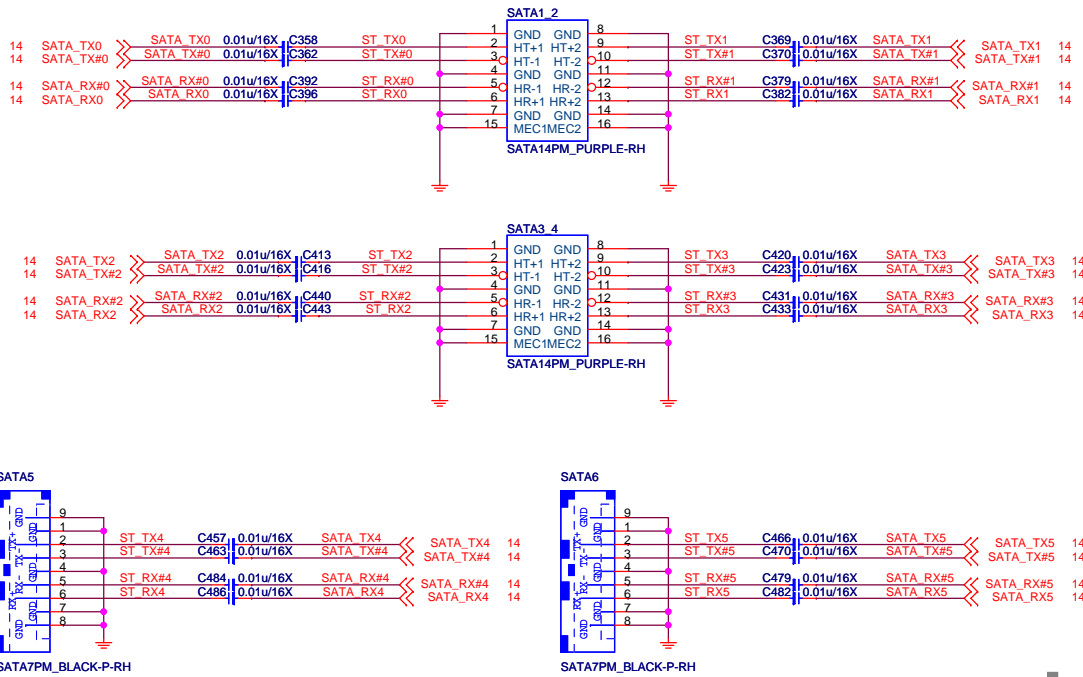
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

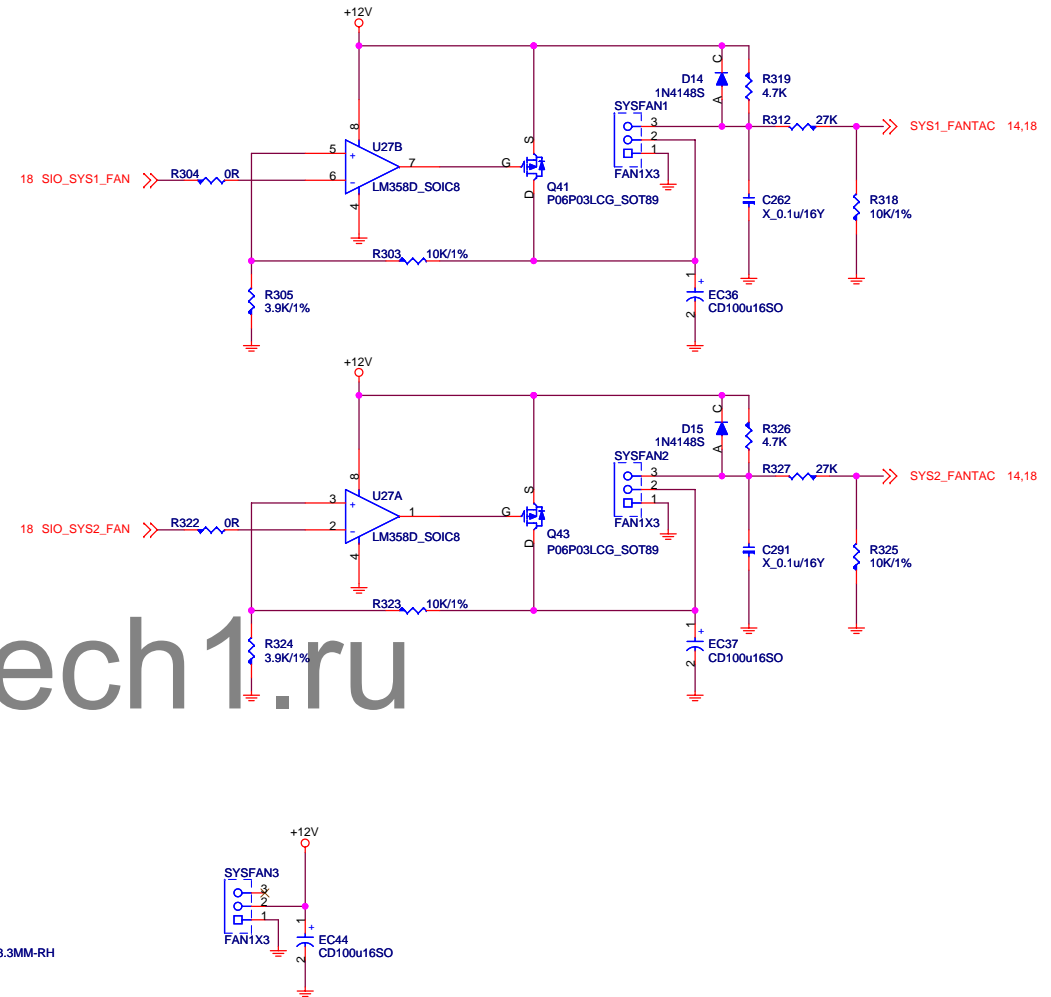
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

MICRO-STAR INT'L CO.,LTD
MS-7635
Size Custom | Document Description **HDMI** | Rev 1.0
Date: Wednesday, November 18, 2009 | Sheet 28 of 47

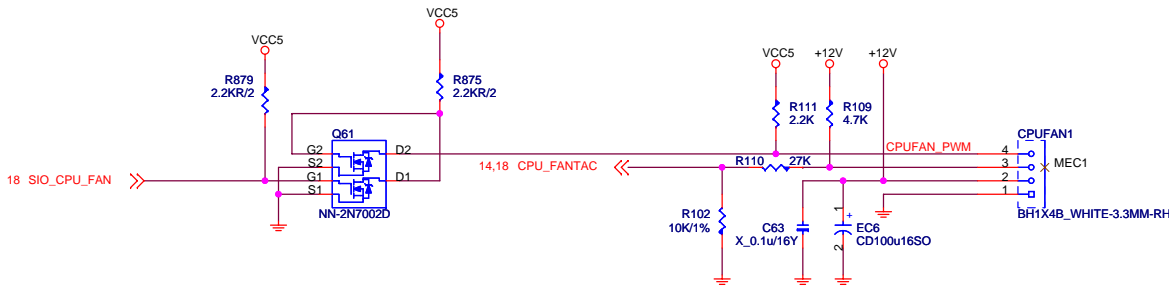
SATA connector (color:Black)



FAN-COUNTROL CIRCUIT



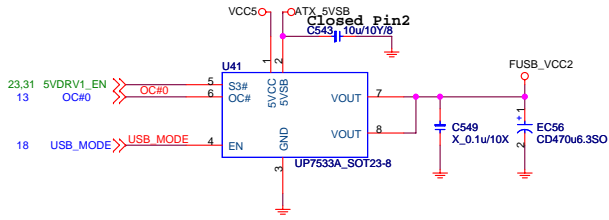
www.aitech1.ru



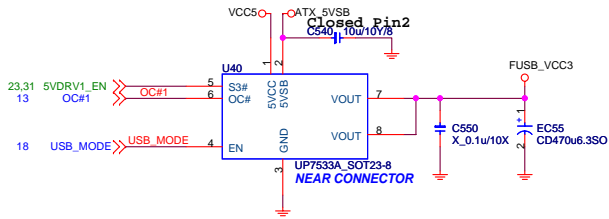
MICRO-STAR INT'L CO.,LTD		
MS-7635		
Size Custom	Document Description	Rev 1.0
SATA Port and Fan Control		
Date: Wednesday, November 18, 2009	Sheet 29 of 47	

Rear USB Connector

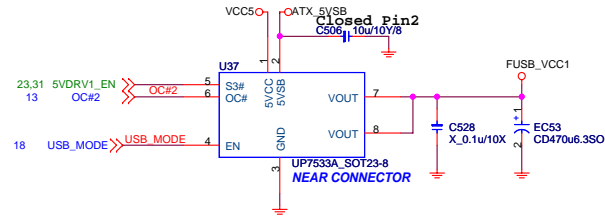
USB POWER FOR PORT 0,1



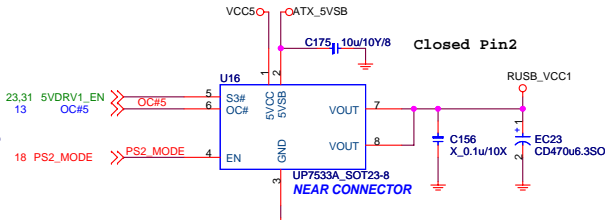
USB POWER REAL PORT 2,3



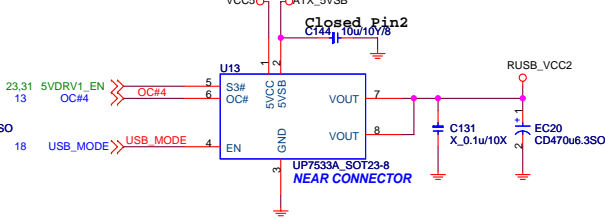
USB POWER FOR PORT 4,5



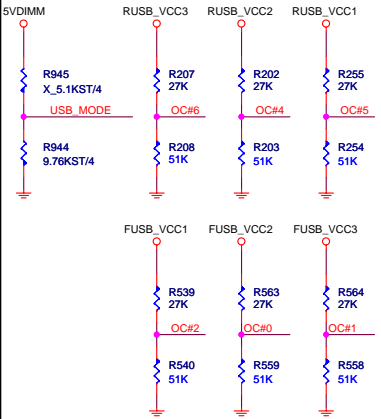
USB POWER FOR PORT 6,7



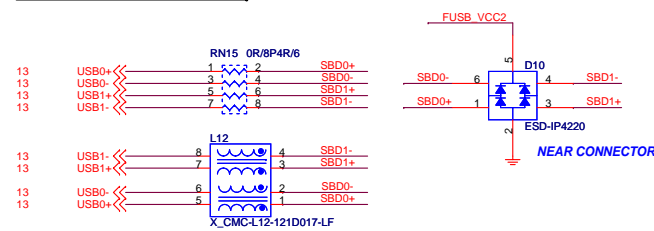
USB POWER FOR PORT 8,9



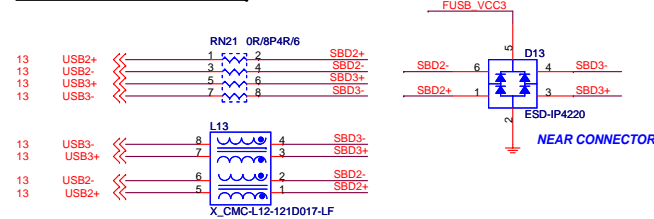
USB_MODE for USB voltage
H: Follow 5VSB
L: Always off



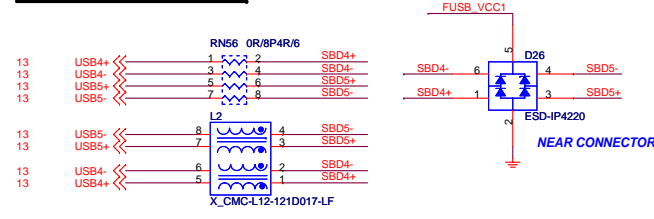
FRONT USB PORT 0,1



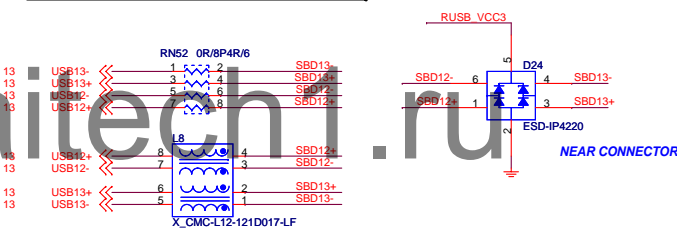
FRONT USB PORT 2,3



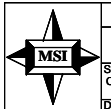
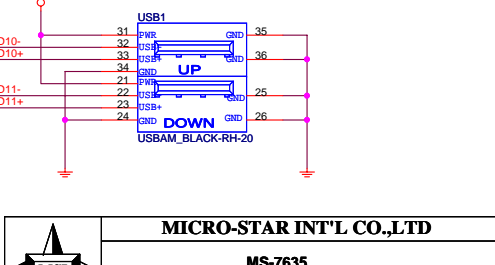
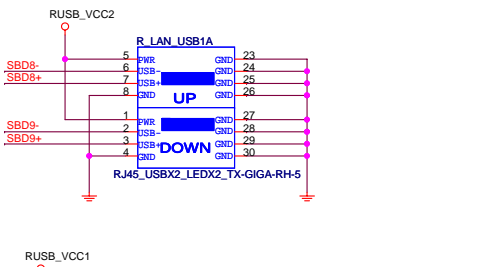
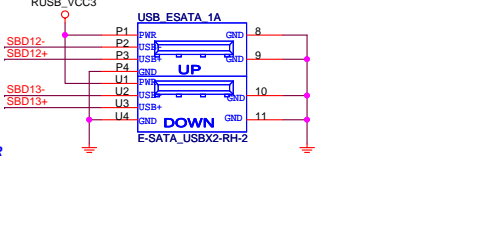
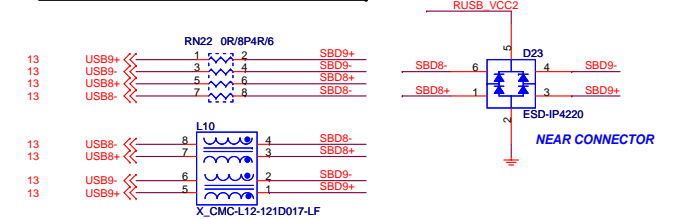
FRONT USB PORT 4,5



REAR USB PORT 6,7 (With 1394)



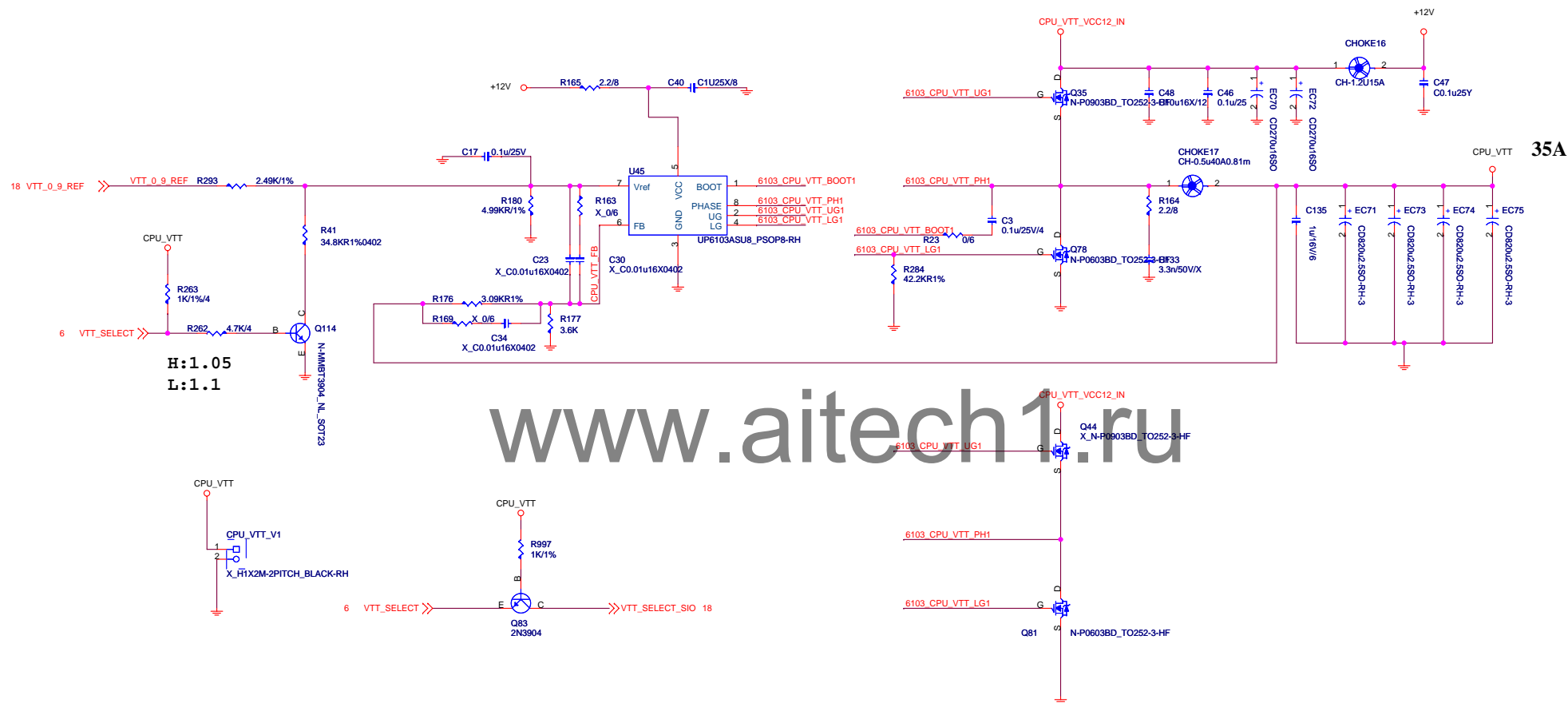
REAR USB PORT 8,9 (With LAN)

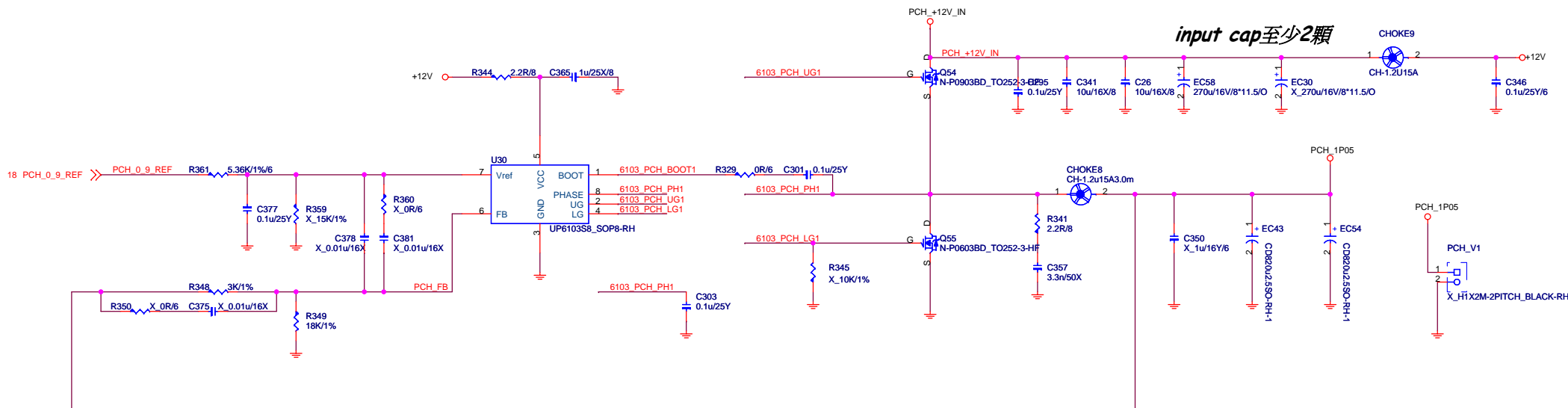


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB Connectors-12port	1.0
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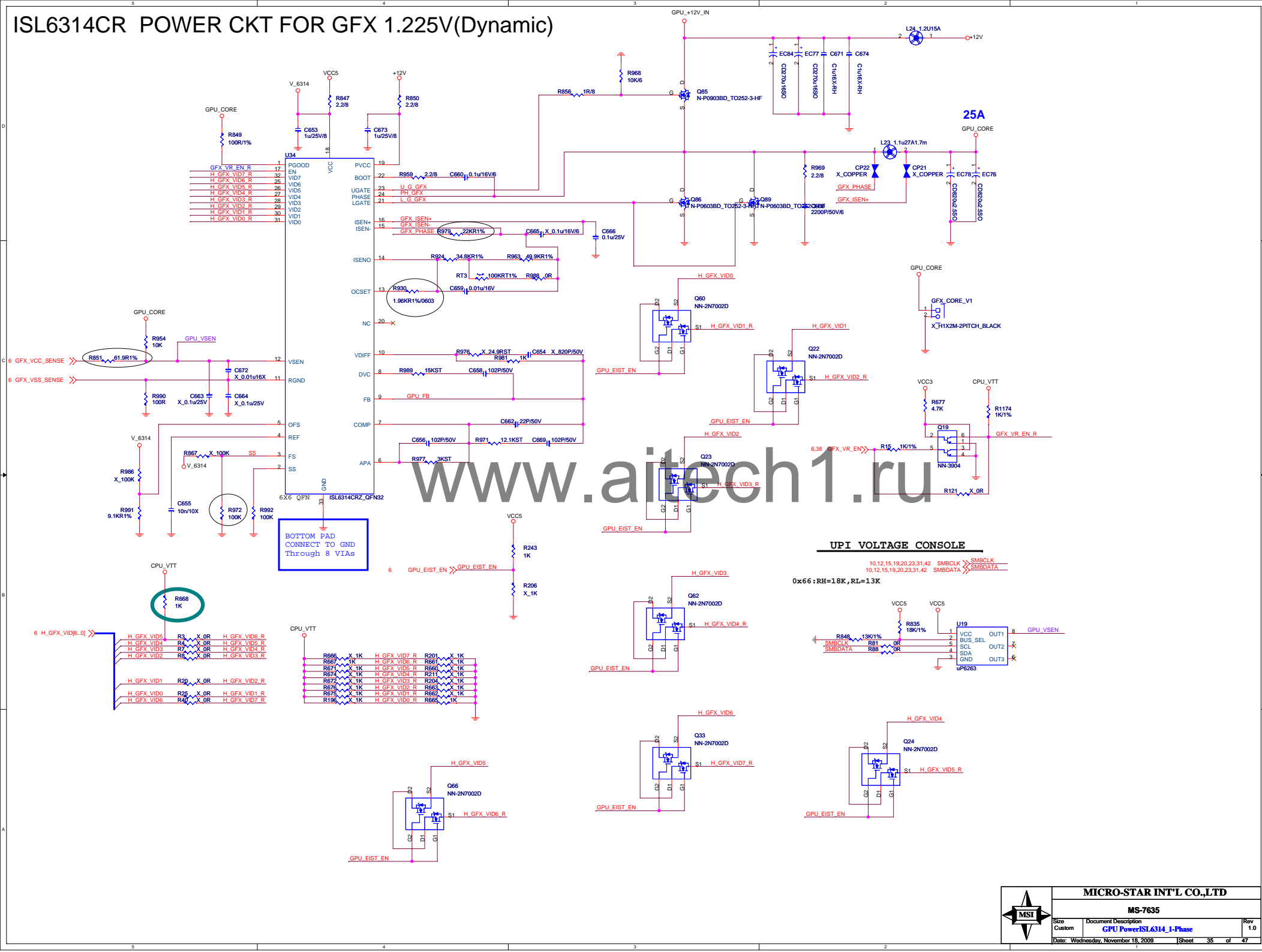


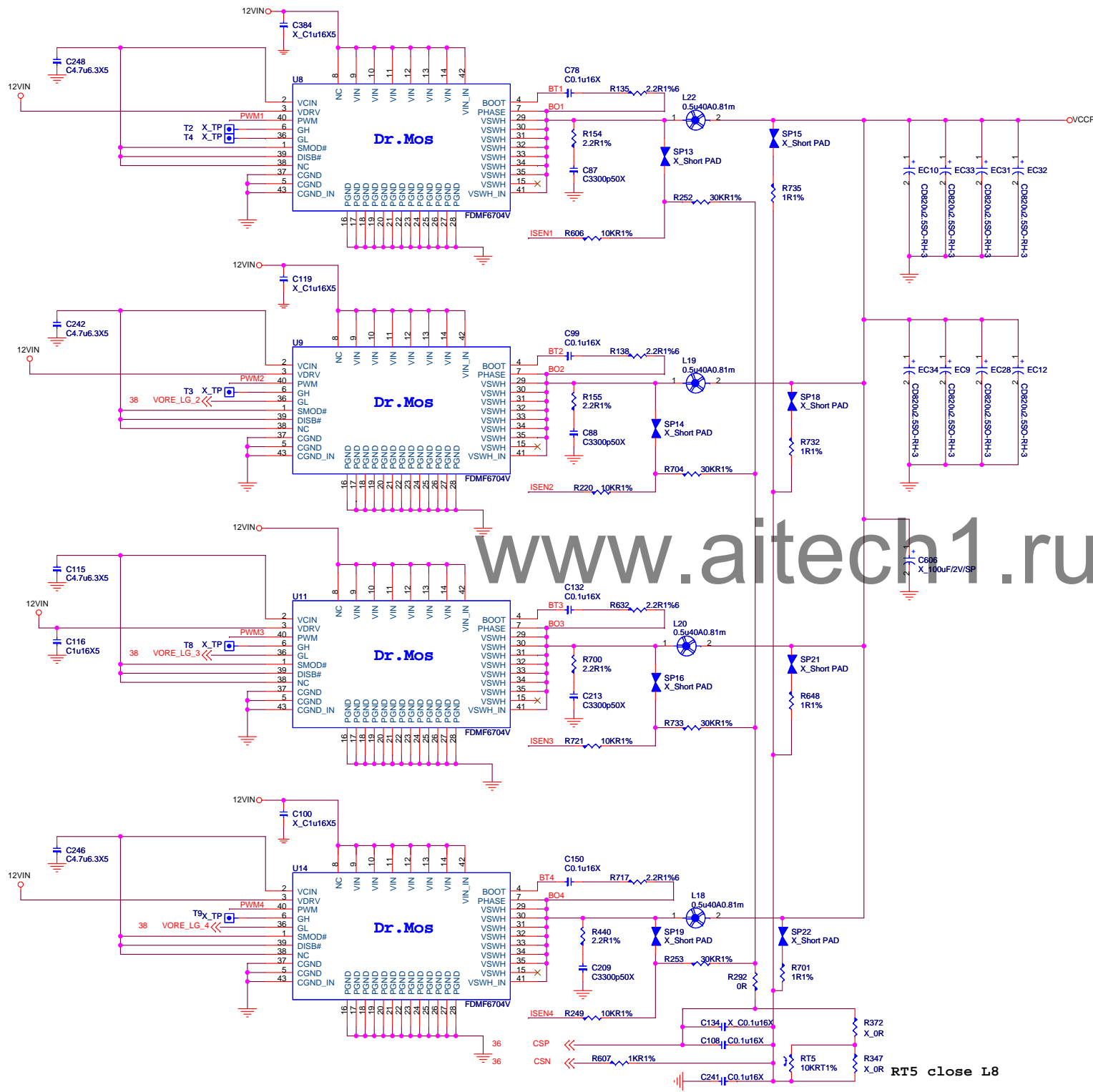
www.aitech1.ru



MICRO-STAR INT'L CO.,LTD			
MS-7635			
Size	Document Description		Rev
Custom	PCH POWER-uP6103 1 Phase		1.0
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ISL6314CR POWER CKT FOR GFX 1.225V(Dynamic)





VCCP

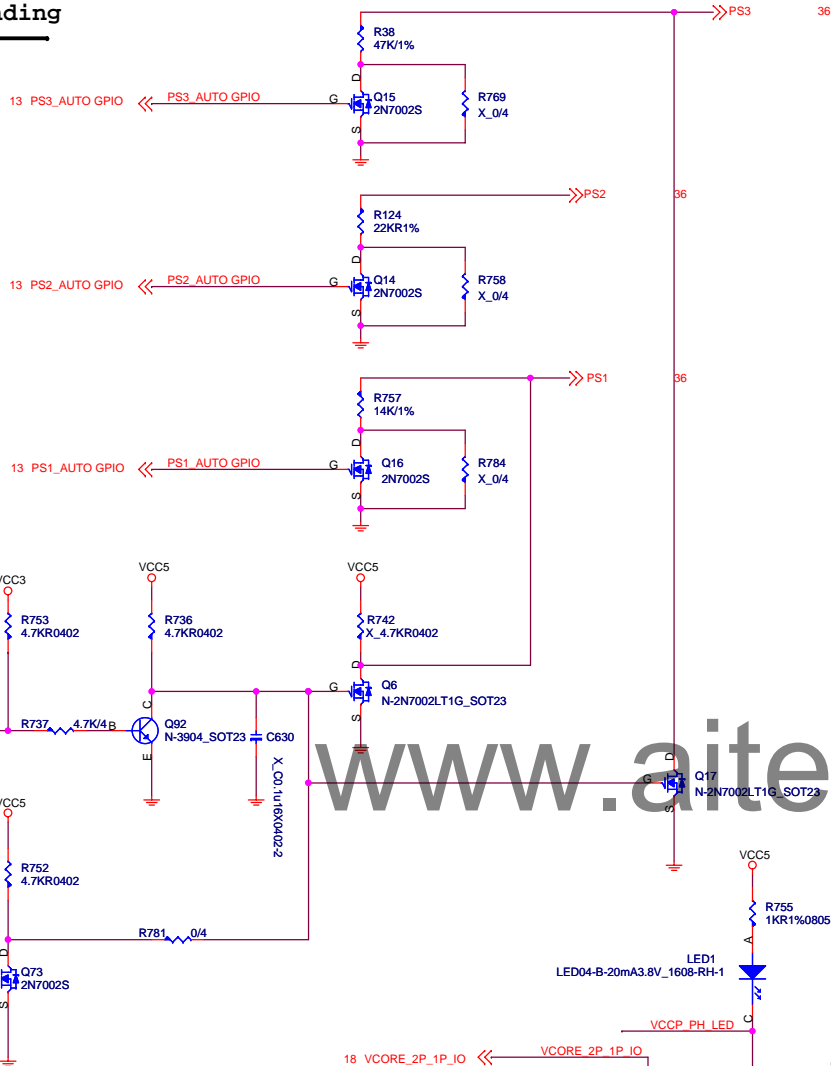
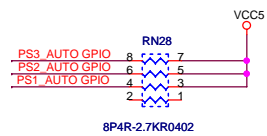
CPU_V1

X_H1X2M-2PITCH_BLACK-RH

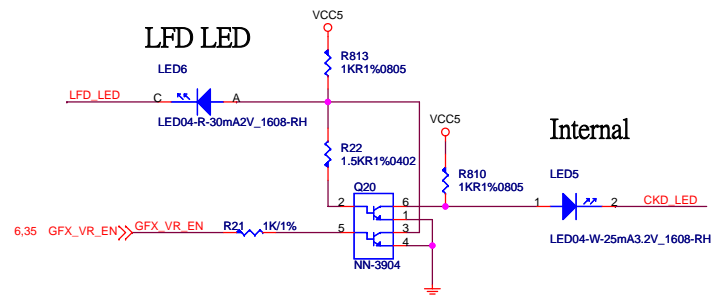
For Power team test only
每項各1顆10u和1u電容)

- PWM1 <--> PWM1 36
- PWM2 <--> PWM2 36
- PWM3 <--> PWM3 36
- PWM4 <--> PWM4 36
- ISEN1 <--> ISEN1 36
- ISEN2 <--> ISEN2 36
- ISEN3 <--> ISEN3 36
- ISEN4 <--> ISEN4 36

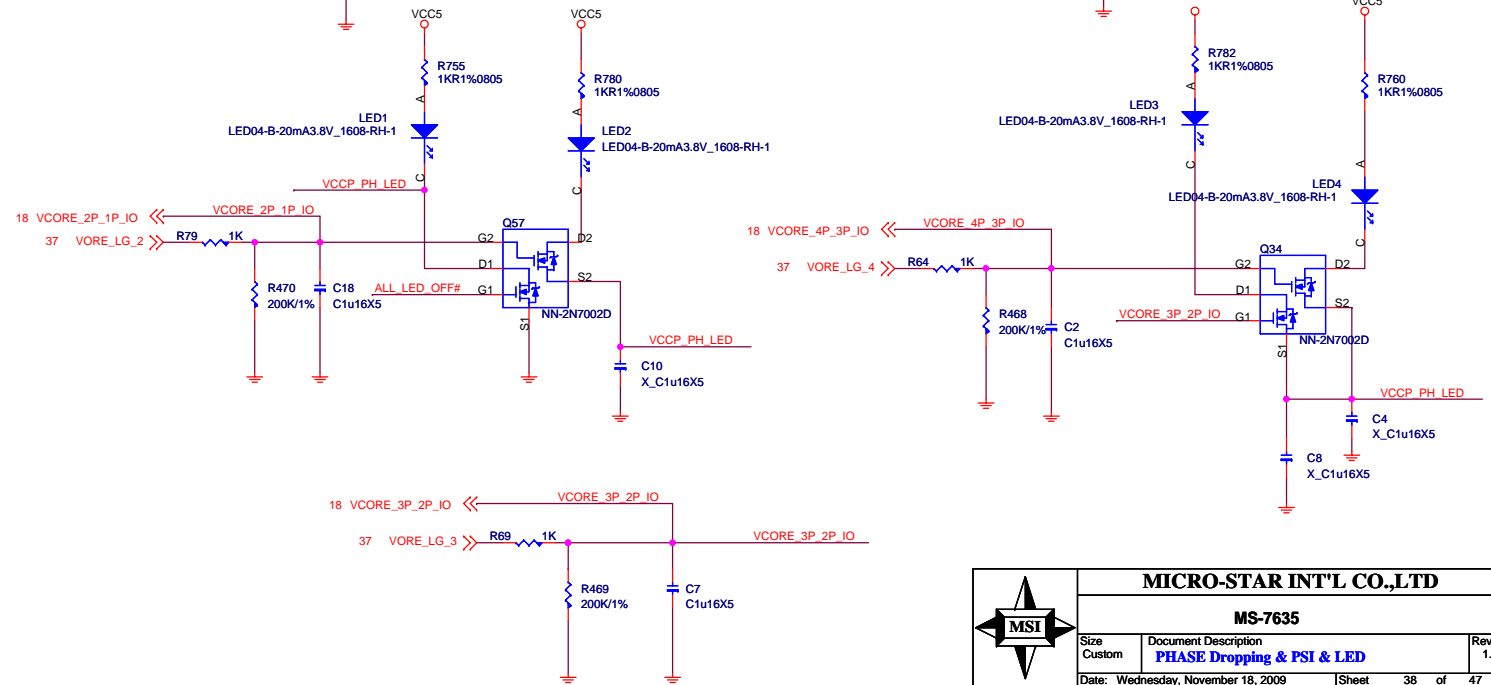
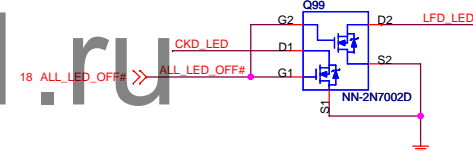
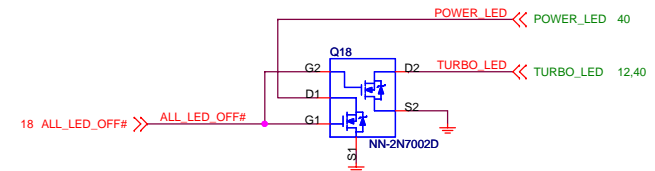
Phase adjustment by loading



CPU type Indicator



all on board LED switch



MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description PHASE Dropping & PSI & LED
----------------	---

Rev	
1.0	

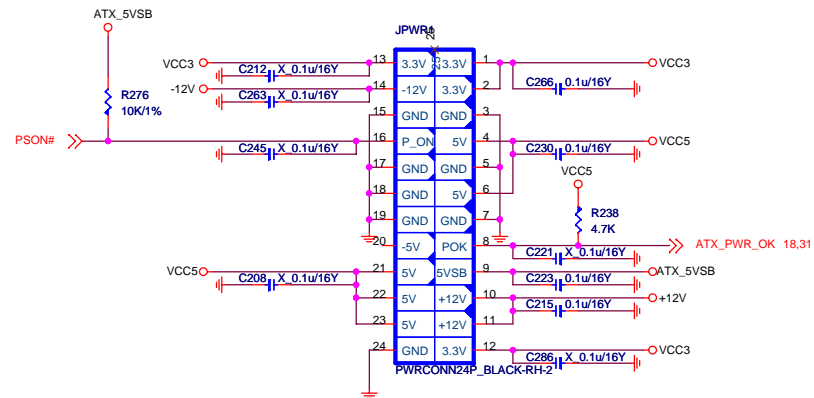
Date: Wednesday, November 18, 2009	Sheet 38 of 47
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touch panel 暫時先移除此SPEC.

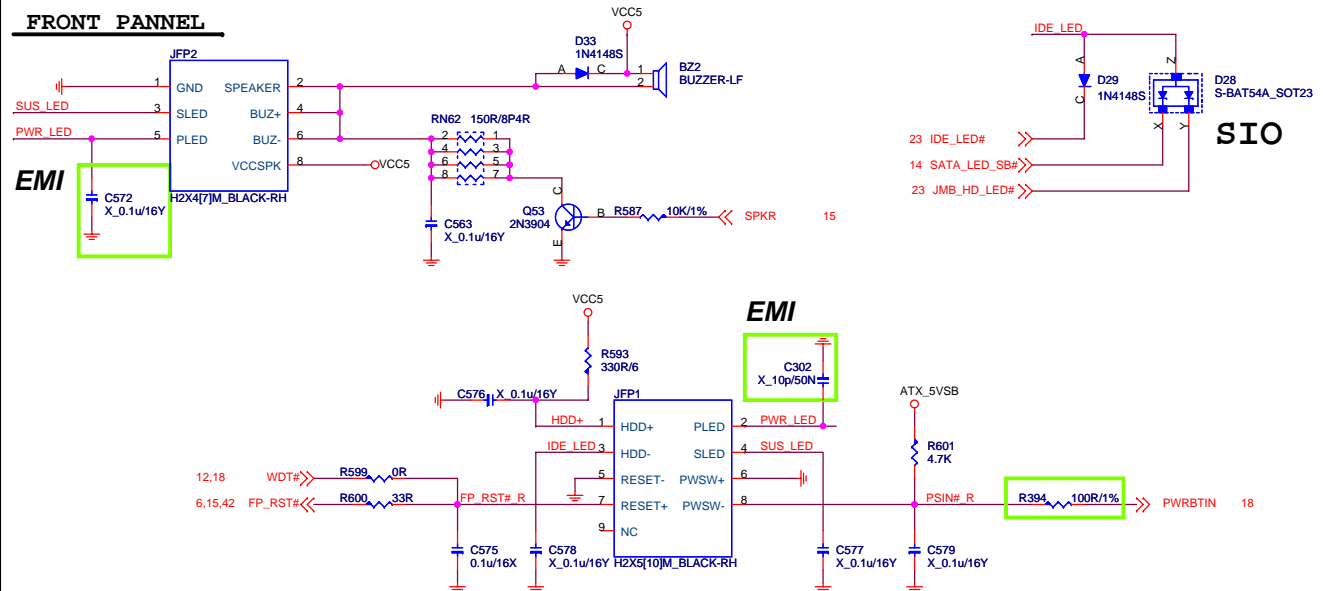
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	MICRO-STAR INT'L CO.,LTD				
	MS-7635				
	Size	Document Description			Rev
	Custom	Touch Pad circuit			1.0
	Date: Tuesday, November 17, 2009			Sheet 39 of 47	

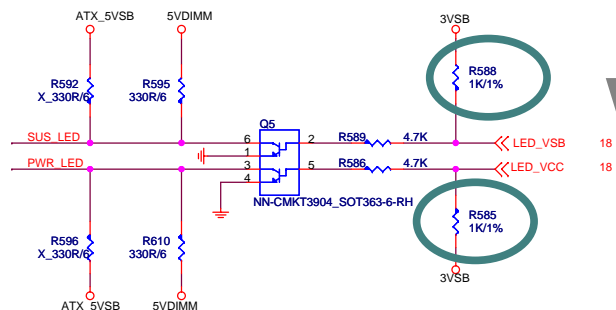
ATX POWER CONNECTOR



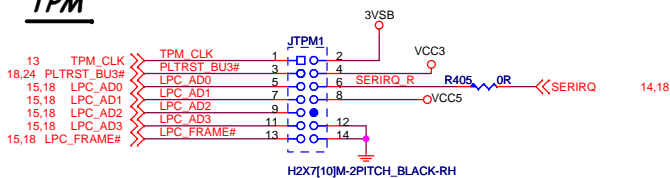
FRONT PANNEL



LED (for Fintek 71889)



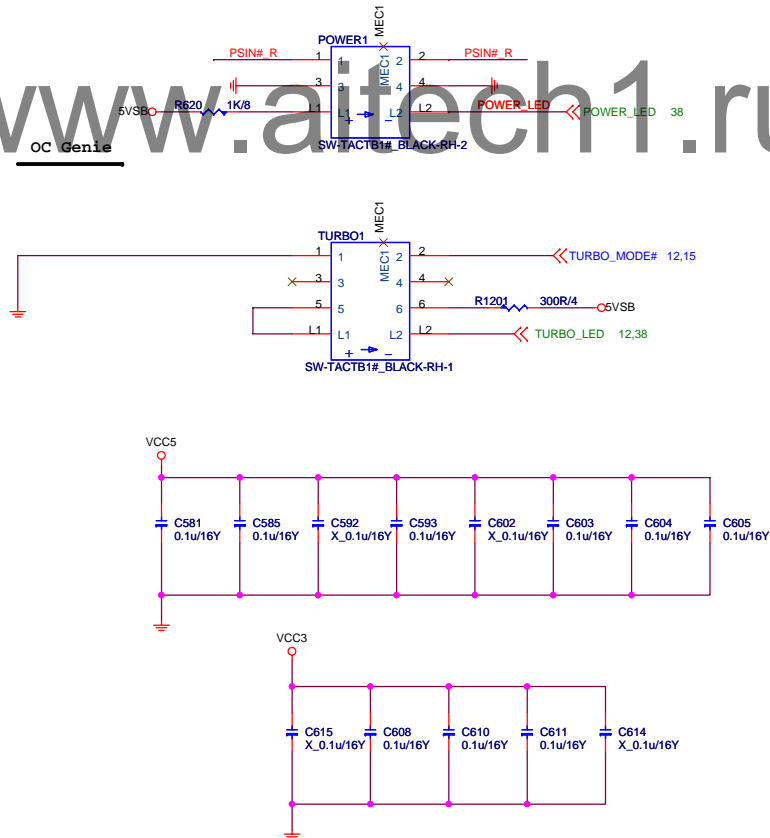
TPM



FOR EMI



Power Button

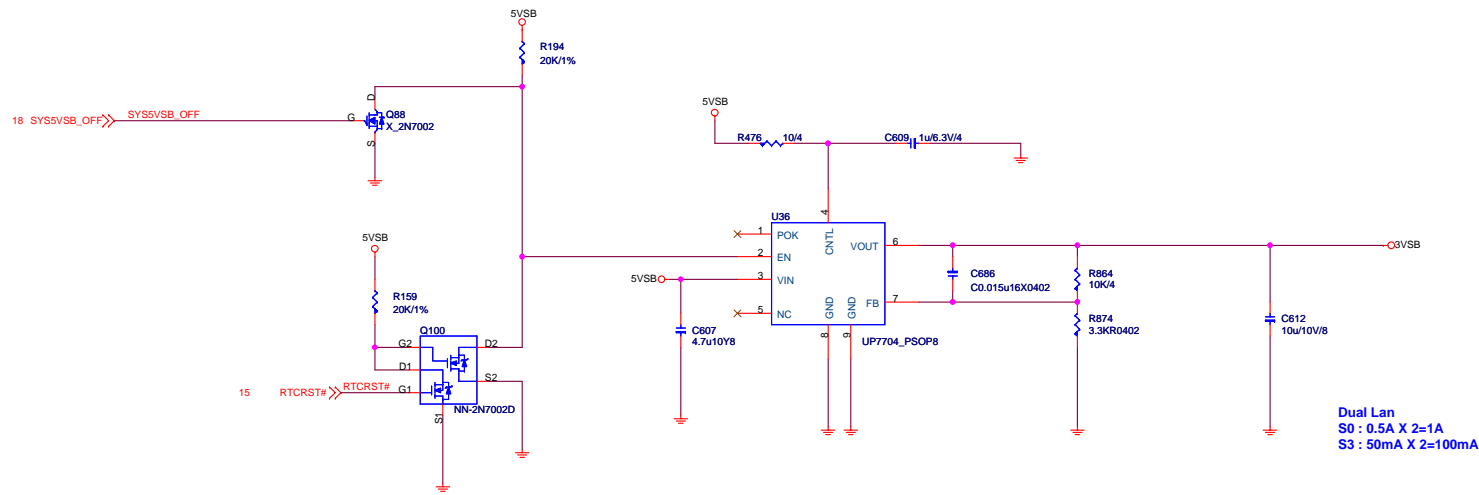


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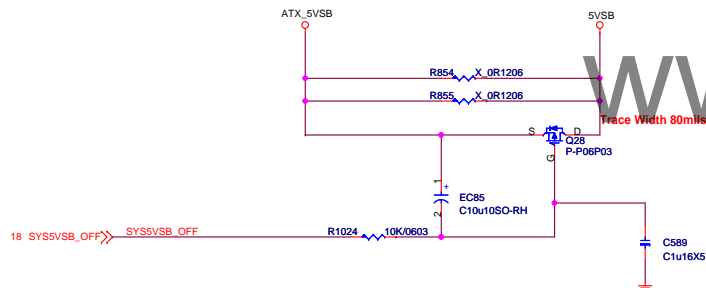
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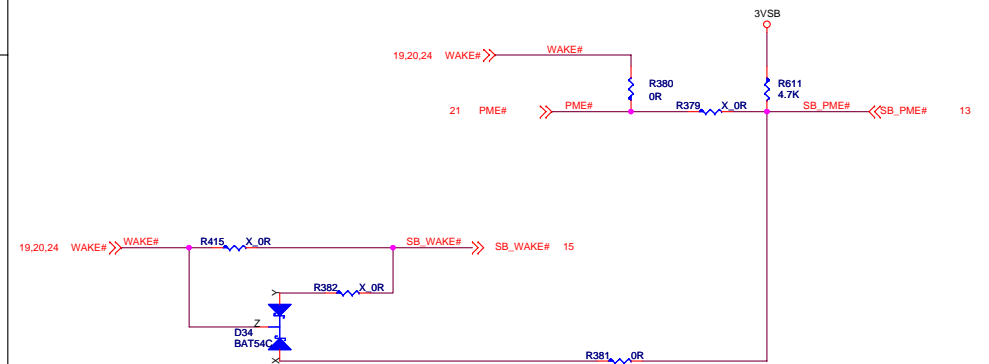
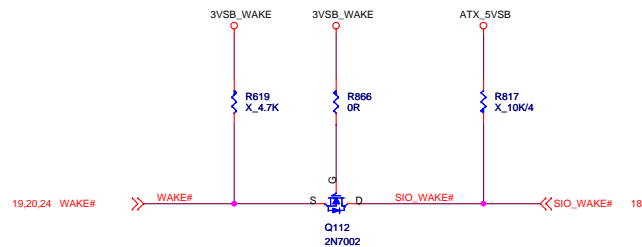
Deep Mode WOL LAN Power CTRL Circuit



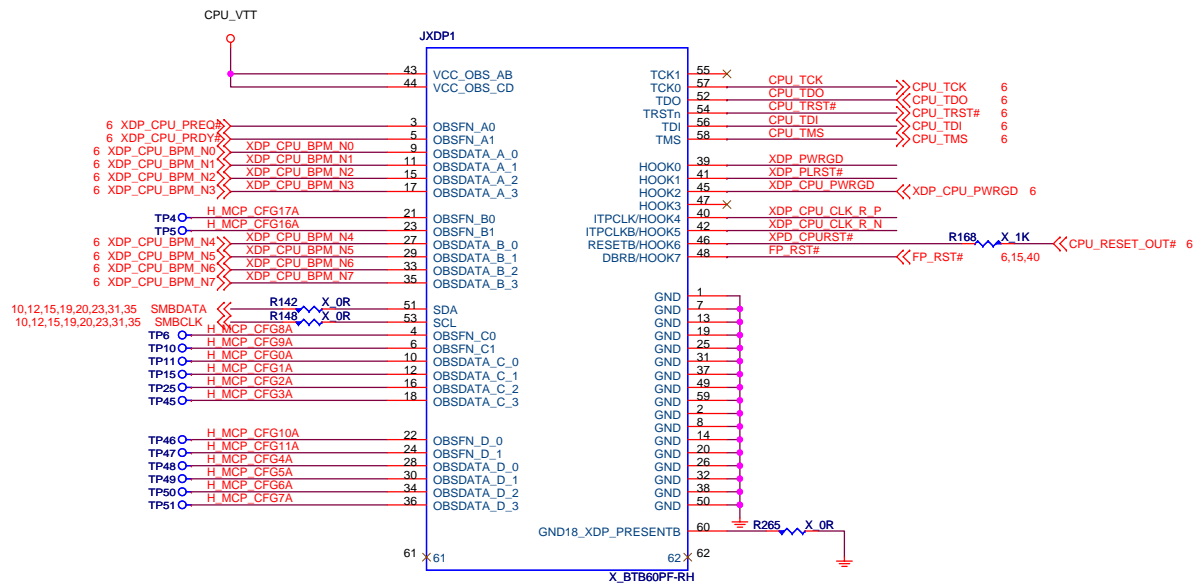
5VSB Power Switch



LAN Wake Up CTRL Circuit



Reserve debug port 5020

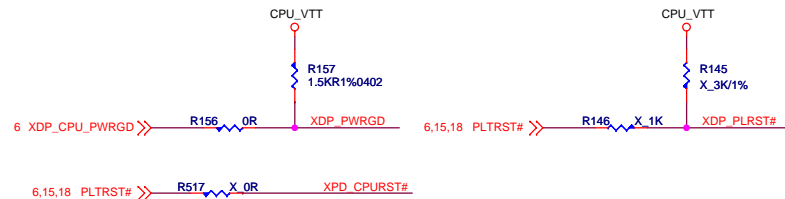


CPU XDP CLOCK

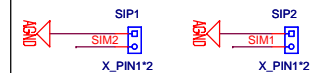
FROM CPU



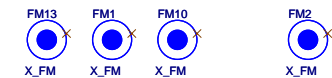
PCH XDP PWRGD/RESET



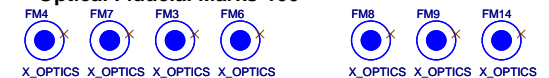
Simulation



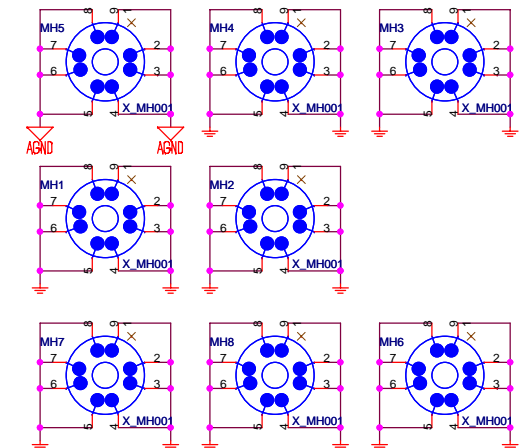
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes

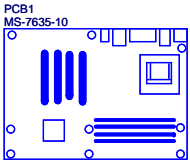


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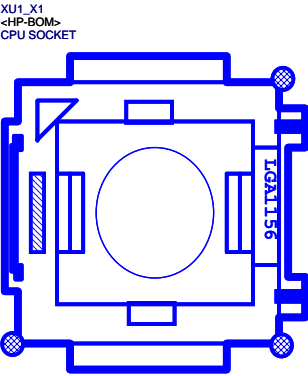
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PCB

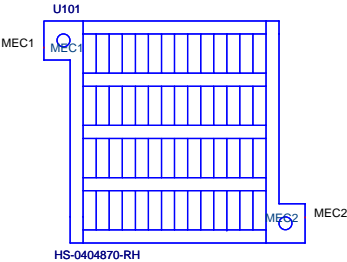


PK0-0763510-G37, 精成,
PK0-0763510-E48, 競華,

CPU SOCKET



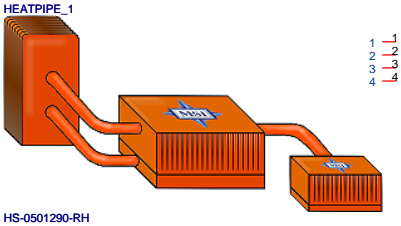
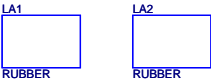
HEATPIPE



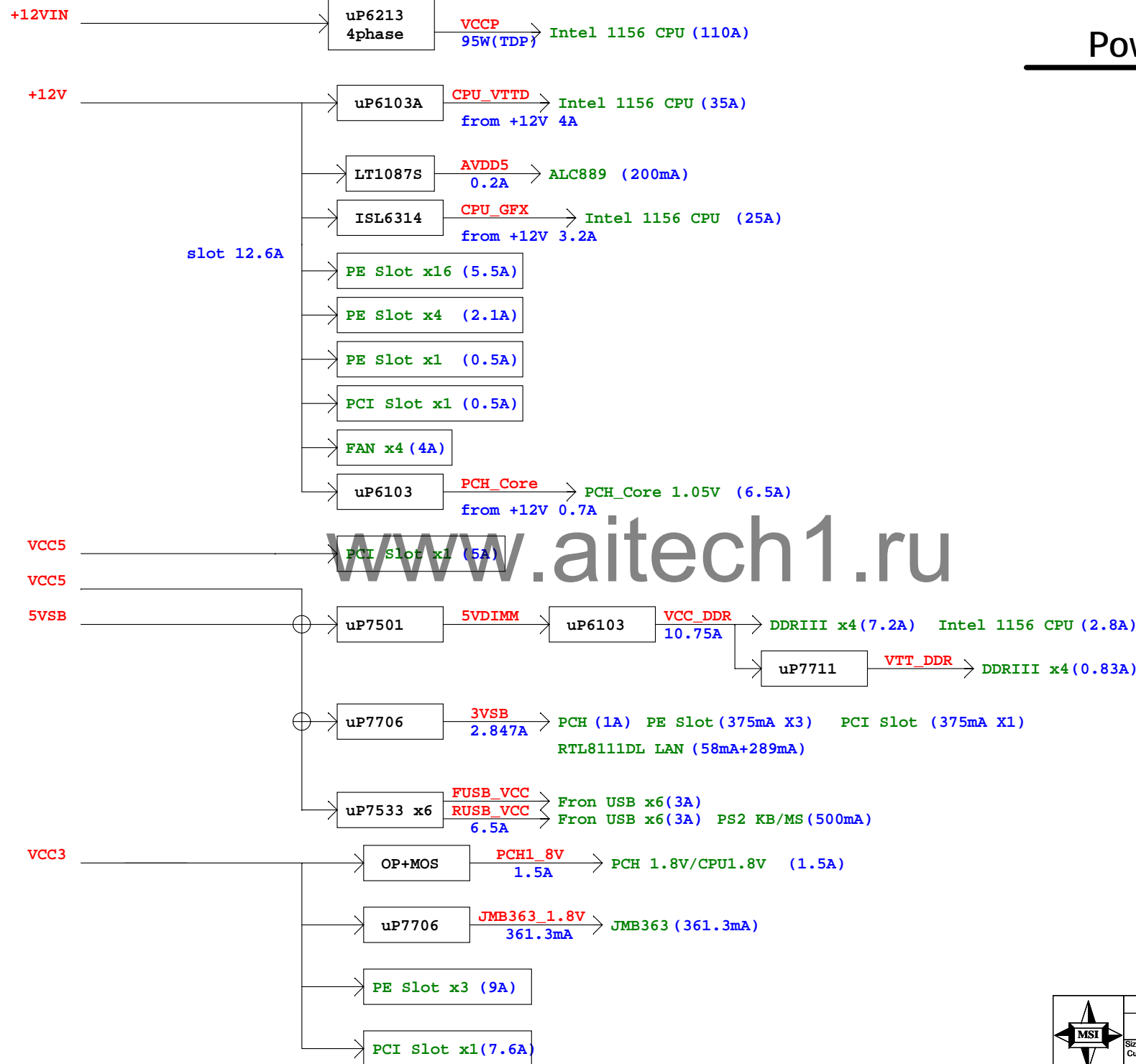
BATTERY



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Power Delivery



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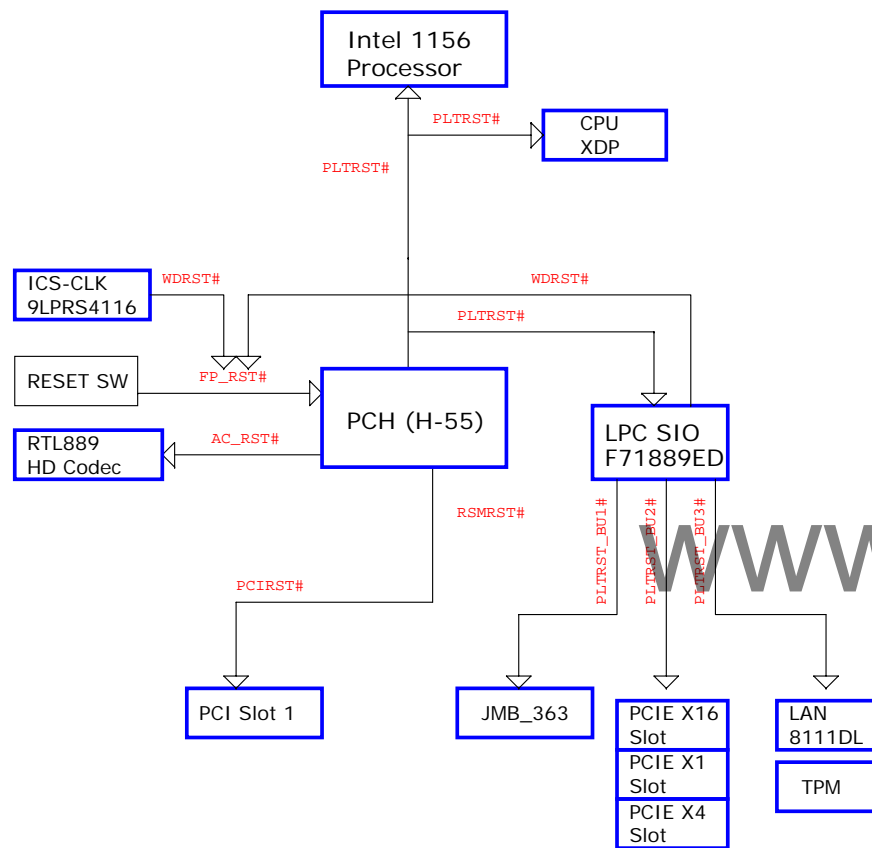
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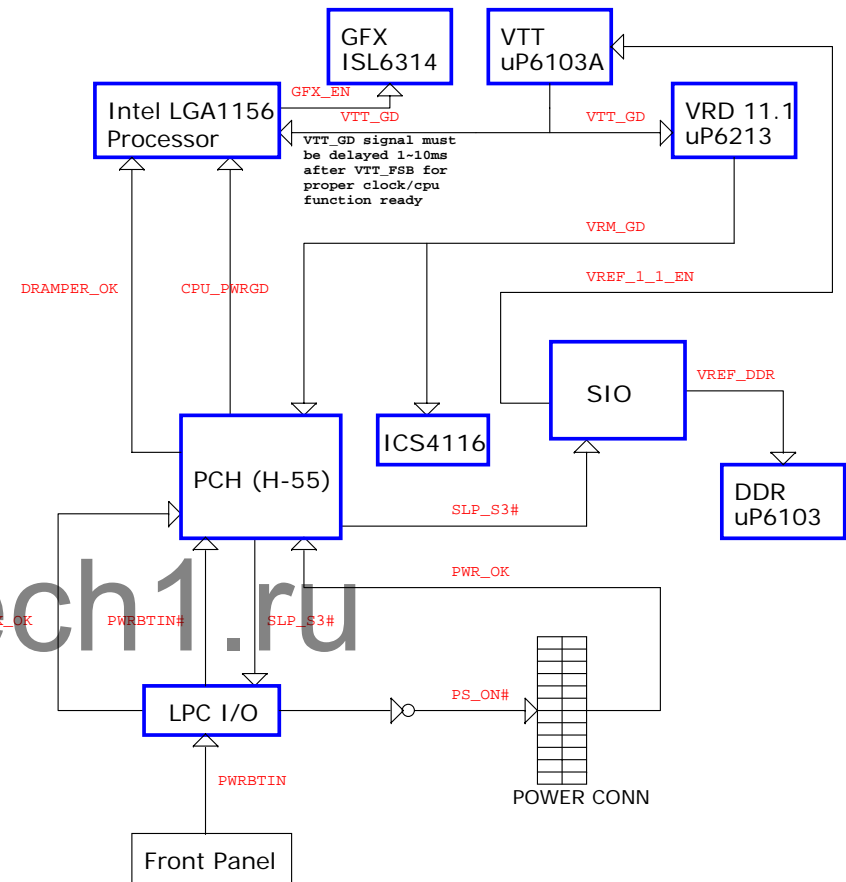
	G3 ---> S5 ---> S0	S0 ---> S3	S3 ---> S0	S0 ---> S5
UP6103	5VSB (PS-->MB) 1-1	5VSB	5VSB	5VSB
	3VSB (By 5VSB) 1-2	3VSB	3VSB	3VSB
	RSMRST# (By SIO to PCH) 1-3 (1-2-->1-3 delay 66ms)	RSMRST#	RSMRST#	RSMRST#
	PWRBTIN# 2-1	PWRBTIN#	PWRBTIN#	PWRBTIN#
	S5# (By PCH to SIO) 2-2	S5#	S5#	4-2 S5# (PCH-->SIO)
	S4# (By PCH to ???) 2-3	S4#	S4#	4-1 S4# (PCH-->???)
	S3# (By PCH to SIO) 2-4	S3# (PCH to SIO) 2-1	S3# (PCH to SIO) 1-1	1-4 S3# (PCH to SIO)
	PSON# (By SIO to PS) 2-5	PSON# (SIO-->ATX) 1-1	PSON# (SIO-->ATX) 1-2	1-6 PSON# (SIO-->ATX)
	12V/5V/3V (By PS to MB) 2-6	12V/5V/3V (ATX-->) 1-2	12V/5V/3V (ATX-->) 1-3	1-7 12V/5V/3V (ATX-->)
OP+MOS	VCC1_8 (By 3V & 12V) 2-7	VCC1_8 (By 3V & 12V) 1-3	VCC1_8 (By 3V & 12V) 1-4	1-9 VCC1_8 (By 3V & 12V)
UP7501	SVDRV1 (By 5V) 2-8 (UP7501 delay 6ms-10ms)	SVDRV1 (By 5V) 1-4	SVDRV1 (By 5V) 1-5	1-8 SVDRV1 (By 5V)
UP6103	VCC_DDR (By 12V) 2-8-1	VCC_DDR	VCC_DDR	1-11 VCC_DDR (By 12V)
	MEM_PWRGD (By PCH to CPU) 2-9 (2-8-1-->2-9 >100ms)	MEM_PWRGD	MEM_PWRGD	1-10 MEM_PWRGD (By PCH to CPU)
UP7711	VTT_DDR (By VCC_DDR) 2-10	VTT_DDR (Ref. VCCS) 1-3	VTT_DDR (Ref. VCCS) 1-6	1-8 VTT_DDR (Ref. VCCS)
UP6103	PCH_1P05 (By SIO PINS#*PCH_0_9_REF*) 2-11	PCH_1P05 (Ref. (SIO PINS#*PCH_0_9_REF*)) 1-7	PCH_1P05 (Ref. (SIO PINS#*PCH_0_9_REF*)) 1-7	1-7 PCH_1P05 (Ref. (SIO PINS#*PCH_0_9_REF*))
UP6103	CPU_VTT (By SIO PINS#*VTT_0_9_REF*) 2-12	CPU_VTT (Ref. (SIO PINS#*PCH_0_9_REF*)) 1-6	CPU_VTT (Ref. (SIO PINS#*PCH_0_9_REF*)) 1-8	1-6 CPU_VTT (Ref. (SIO PINS#*PCH_0_9_REF*))
	VTT_PGD (By CPU_VTT to CPU/UP6314) 2-13 (2-12-->2-13 Delay 100ms-500ms)	VTT_PGD (S3# to VTT_PGD) 1-2	VTT_PGD (S3# to VTT_PGD) 1-9	1-5 VTT_PGD (S3# to VTT_PGD)
	GFX_VR_EN (By CPU to UP6314) 2-14	GFX_VR_EN (By CPU to UP6314) 1-3	GFX_VR_EN (By CPU to UP6314) 1-10	1-8 GFX_VR_EN (By CPU to UP6314)
UP6314	GPU_CORE (By GFX_VR_EN) 2-15	GPU_CORE (By GFX_VR_EN) 1-7	GPU_CORE (By GFX_VR_EN) 1-11	1-9 GPU_CORE (By GFX_VR_EN)
UP6213	VCCP (By VTT_PGD) 2-16 0.05-650ms	VCCP (By VTT_PGD to Vccp) 1-3	VCCP (By VTT_PGD to Vccp) 1-12	1-6 VCCP (By VTT_PGD to Vccp)
	VRM_PGD (By Vccp) 2-17 (2-7-->2-17 >1ms) (2-1-->2-17 >2-9-->2-17 >1ms) >0.0-650ms	VRM_PGD (By Vccp) 1-4	VRM_PGD (By Vccp) 1-13	1-7 VRM_PGD (By Vccp)
	CK_PGD (By VRM_PGD) 2-18	CK_PGD (By VRM_PGD) 1-5	CK_PGD (By VRM_PGD) 1-14	1-8 CK_PGD (By VRM_PGD)
	ATX_POK (By 12V/5V/3V Delay 100ms-500ms) 2-19	ATX_POK (By PSON#) 1-3	ATX_POK (By PSON#) 1-15	1-8 ATX_POK (By PSON#)
	CHIP_PGD (By ATX_POK & 3V SIO to PCH) 2-20 (2-6-->2-20 delay 400ms)	CHIP_PGD (By 3V & ATX_POK SIO to PCH) 1-3	CHIP_PGD (By 3V & ATX_POK SIO to PCH) 1-16	1-12 CHIP_PGD (By 3V & ATX_POK SIO to PCH)
	CPUPWROK (PCH to CPU) 2-21	CPUPWROK (PCH to CPU) 1-3	CPUPWROK (By PCH to CPU) 1-17	1-3 CPUPWROK (By PCH to CPU)
	PLTRST# (By PCH to CPU) 2-22	PLTRST# (By PCH to CPU) 1-1	PLTRST# (PLTRST#) 1-18	1-1 PLTRST# (PLTRST#)
	CPURST# (By PLTRST#) 2-23	CPURST# (By PLTRST# to CPURST#) 1-2	CPURST# (By PLTRST# to CPURST#) 1-19	1-2 CPURST# (By PLTRST# to CPURST#)

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RESET MAP



PWROK MAP

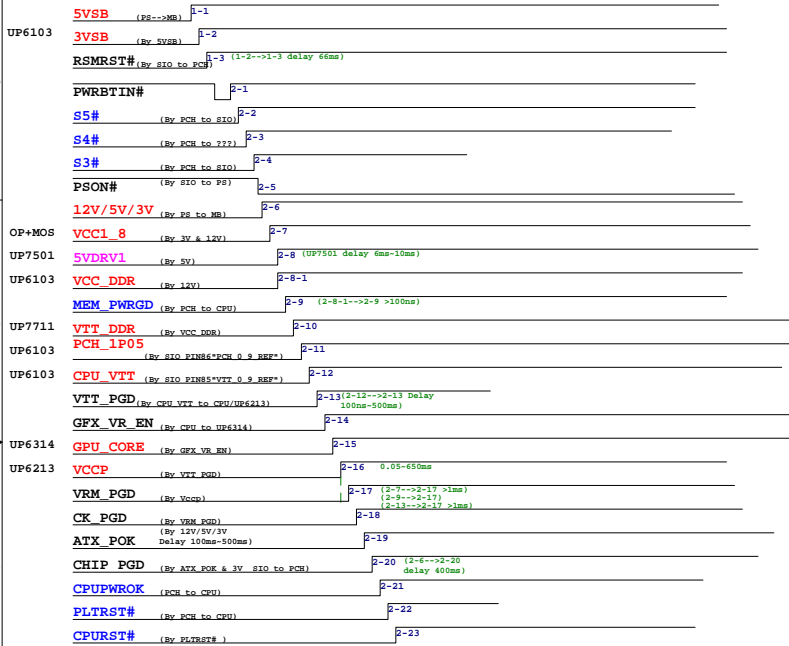


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G3 ---> S5 ---> S0



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Date

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